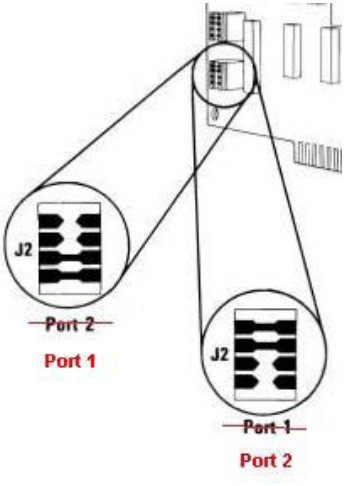
November 2011

IMPORTANT

1. Page 20 contains an error - the jumper positions for the parallel port are incorrectly shown. The correct positions are shown below in red.



2. As verified by the schematic diagram, I/O address usage and interrupt usage is as follows:

   Serial port 1 = I/O base address 3F8 and interrupt 4
   Serial port 2 = I/O base address 2F8 and interrupt 3

   Parallel port 1 = I/O base address 378 and interrupt 7
   Parallel port 2 = I/O base address 278 and interrupt 5

Personal Computer Hardware Reference Library

Serial/Parallel Adapter

Contents

Notes:

Description

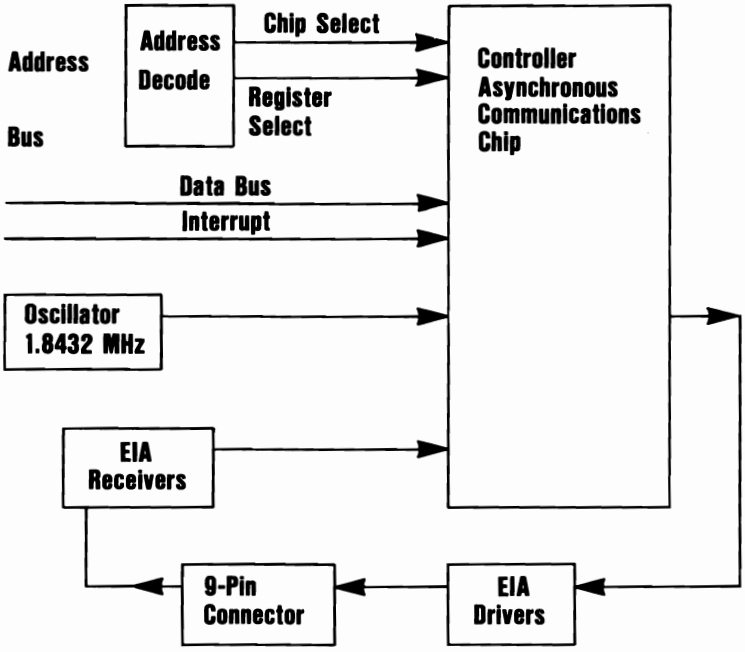
The IBM Personal Computer AT Serial/Parallel Adapter provides a parallel port and a serial port. It plugs into a system-board expansion slot. All system-control signals and voltage requirements are provided through a 2- by 31-position card edge connector.

Serial Portion of the Adapter

The serial portion of the adapter is fully programmable and supports asynchronous communications. It will add and remove start, stop, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. Five-, six-, seven- and eight-bit characters with 1, 1.5, or 2 stop bits are supported. A prioritized interrupt system controls transmit, receive, error, and line status as well as data-set interrupts.

The rear of the adapter has a 9-pin D-shell connector that is classified as an RS-232C port. When the optional IBM Communications Cable (9-Pin), which has a 9-pin D-shell connector on one end and a 25-pin D-shell connector on the other end, is connected to the adapter, the 25-pin end of the cable has all the signals of a standard EIA RS-232C interface.

The following figure is a block diagram of the serial portion of the adapter.



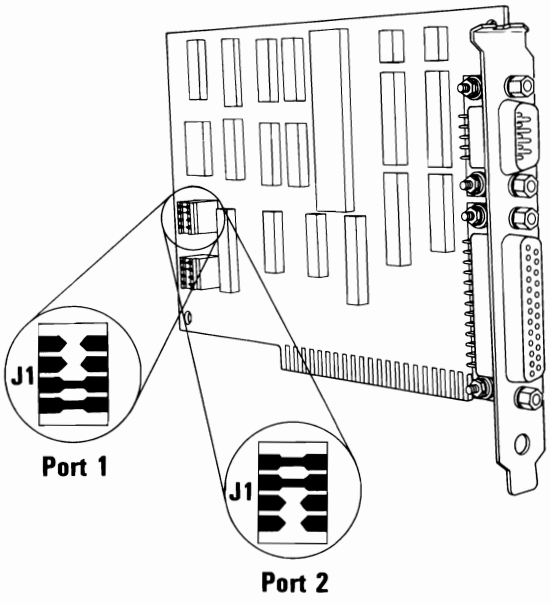
Serial Portion Block Diagram

The serial portion of the adapter has a controller that provides the following functions:

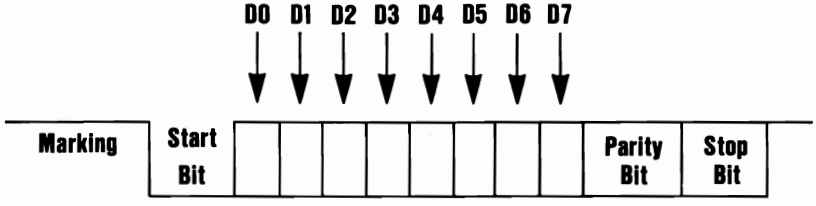
- Adds or deletes standard, asynchronous-communications bits to or from a serial data stream.
- Provides full, double buffering, which eliminates the need for precise synchronization.
- Provides a programmable baud-rate generator.
- Provides modem controls (CTS, RTS, DSR, DTR, RI, and CD).

Communications Application

The serial output port may be addressed as either communications port 1 or communications port 2 as defined by jumper J1 (see the following figure). In this section hex addresses begin with an X which can be either a 3 for communications port 1 (interrupt level 4) or a 2 for communications port 2 (interrupt level 3).



The data format will be as follows:



Bit 0 is the first data bit to be sent or received. The controller automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bit (1, 1.5, or 2, depending on the command in the line-control register).

Controller Specifications

The following describes the function of controller input/output signals.

Input Signals

-Clear to Send: (-CTS), Pin 36—The '-CTS' signal is a modem-control function input, the condition of which can be tested by the processor by reading bit 4 (-CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates if the '-CTS' input has changed state since the previous reading.

> **Note:** Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

-Data Set Ready: (-DSR), Pin 37—When low, indicates the modem or data set is ready to establish the communications link and transfer data with the controller. The '-DSR' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 5 (-DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates if the '-DSR' input has changed since the previous reading.

> **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

-Data Carrier Detect: (-DCD), Pin 38—When low, indicates the modem or data set detected a data carrier. The '-DCD' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 7 (-DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates if the '-DCD' input has changed state since the previous reading.

> **Note:** Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Ring Indicator: (-RI), Pin 39—When low, indicates the modem or data set detected a telephone ringing signal. The '-RI' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 6 (-RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates if the '-RI' input has changed from an active to an inactive state since the previous reading.

> **Note:** Whenever the RI bit of the modem status register changes from an inactive to an active state, an interrupt is generated if the modem-status interrupt is enabled.

VCC Pin 40—+5 Vdc supply

VSS Pin 20—Ground (0 Vdc) reference

Output Signals

-Data Terminal Ready: (-DTR), Pin 33—When active, informs the modem or data set that the controller is ready to communicate. The '-DTR' output signal can be set to an active level by programming bit 0 (-DTR) of the modem control register to an active level. The '-DTR' signal is set inactive upon a master reset operation.

-Request to Send: (-RTS), Pin 32—When active, informs the modem or data set that the controller is ready to send data. The '-RTS' output signal can be set to an active level by programming bit 1 (-RTS) of the modem control register to an active level. The '-RTS' signal is set inactive upon a master reset operation.

-Output 1: (-OUT 1), Pin 34—User-designated output that can be set to an active level by programming bit 2 (-OUT 1) of the modem control register to an inactive level. The '-OUT 1' signal is set inactive upon a master reset operation. Pin 34 is connected to an active source.

-Output 2: (-OUT 2), Pin 31—User-designated output that can be set to an active level by programming bit 3 (-OUT 2) of the modem control register to an inactive level. The '-OUT 2' signal is set inactive upon a master reset operation. Pin 31 controls interrupts to the system.

Controller-Accessible Registers

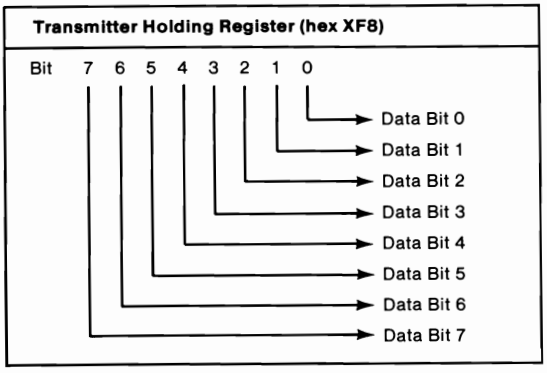
The controller has a number of accessible registers. The system programmer may gain access to or control any of the controller registers through the microprocessor. These registers are used to control the controller's operations and to transmit and receive data. The X in the register address determines the the port selected; 3 is for port 1 and 2 is for port 2.

Specific registers are selected according to the following figure:

I/O Address	Register Selected	DLAB State
XF8	TX Buffer	0 (Write)
XF8	RX Buffer	0 (Read)
XF8	Divisor Latch LSB	1
XF9	Divisor Latch MSB	1
XF9	Interrupt Enable Register	0
XFA	Interrupt Identification Register	
XFB	Line Control Register	
XFC	Modem Control Register	
XFD	Line Status Register	
XFE	Modem Status Register	
XFF	Reserved	

Controller-Accessible Registers

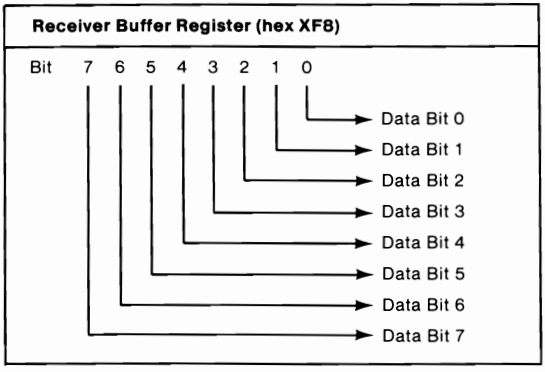
Transmitter Holding Register (hex XF8): The transmitter holding register (THR) contains the character to be sent.



Transmitter Holding Register

Bit 0 is the least-significant bit and the first bit sent serially.

Receiver Buffer Register (hex XF8): The receiver buffer register (RBR) contains the received character.

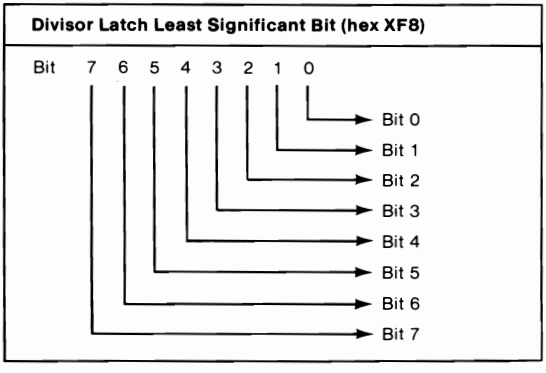


Receiver Buffer Register

Bit 0 is the least-significant bit and the first bit received serially.

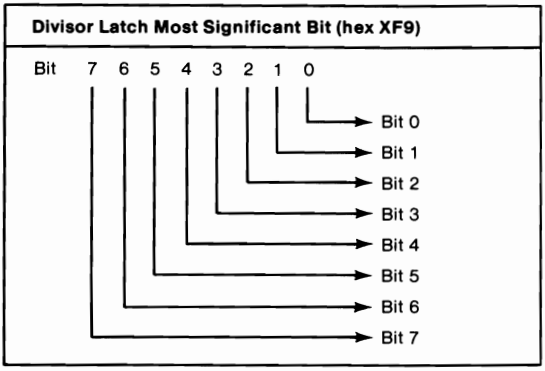
Programmable Baud-Rate Generator: The controller has a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Divisor Latch LSB (hex XF8)



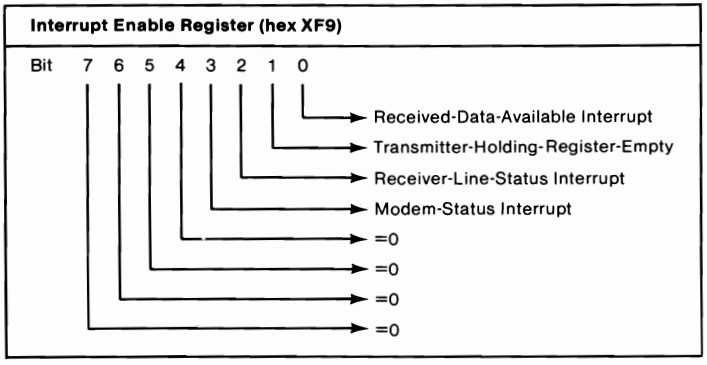
Divisor Latch Least Significant Bit

Divisor Latch MSB (hex XF9)



Divisor Latch Most Significant Bit

Interrupt Enable Register (hex XF9): This 8-bit register allows the four types of controller interrupts to separately activate the 'chip-interrupt' (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, by setting the appropriate bits of this register to logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the 'IER' and the active 'INTRPT' output from the chip. All other system functions operate normally, including the setting of the line-status and modem-status registers.



Interrupt Enable Register

Bit 0 When set to logical 1, enables the received-data-available interrupt.

Bit 1 When set to logical 1, enables the transmitter-holding-register-empty interrupt.

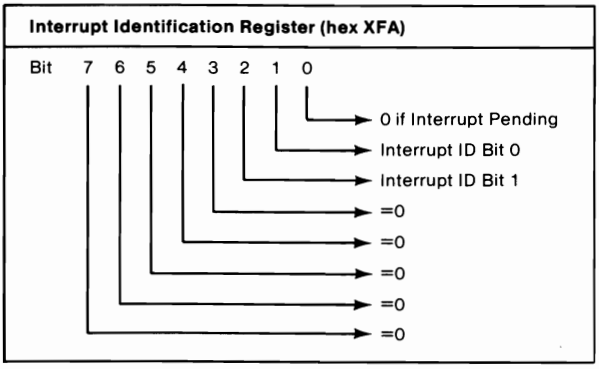
Bit 2 When set to logical 1, enables the receiver-line-status interrupt.

Bit 3 When set to logical 1, enables the modem-status interrupt.

Bits 4–7 These four bits are always logical 0.

Interrupt Identification Register (hex XFA): The controller has an on-chip interrupt capability that makes communications possible with all of the currently popular microprocessors. In order to minimize programming overhead during data character transfers, the controller prioritizes interrupts into four levels: receiver-line-status (priority 1), received-data-available (priority 2), transmitter-holding-register-empty (priority 3), and modem status (priority 4).

Information about a pending prioritized interrupt is stored in the interrupt identification register (IIR). (See the figure "Interrupt Control Functions," later.) The IIR, when addressed during chip-select time, stops the pending interrupt with the highest priority, no other interrupts are acknowledged until the processor services that interrupt.



Interrupt Identification Register

Bit 0 This bit can be used in either hard-wired, prioritized, or polled conditions to indicate if an interrupt is pending. When bit 0 is logical 0, an interrupt is pending, and the IIR contents may be used as a

pointer to the appropriate interrupt service routine. When bit 0 is logical 1, no interrupt is pending, and polling (if used) continues.

Bits 1–2 These two bits identify the pending interrupt that has the highest priority, as shown in the following figure:

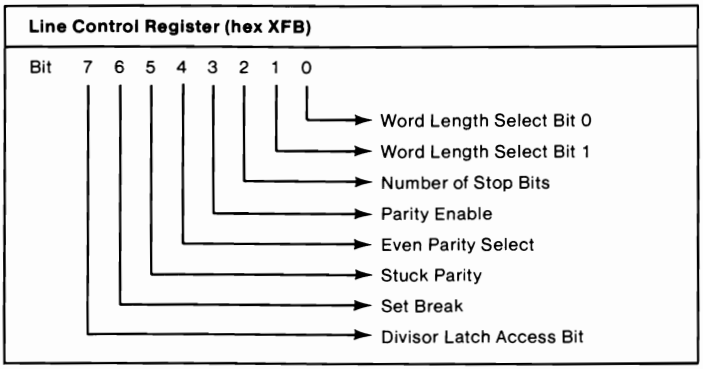
Interrupt ID Register			Interrupt Set And Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or writing into the THR
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Interrupt Priority

Bits 3–7 These five bits are always logical 0.

Line-Control Register (hex XFB): The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to

controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need to store line characteristics separately in system memory.



Line Control Register

Bits 0, 1 These two bits specify the number of bits in each serial character that is sent or received. The encoding of bits 0 and 1 is as follows:

Bit 0	Bit 1	Word Length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

Word Length

Bit 2 This bit specifies the number of stop bits in each serial character that is sent or received. If bit 2 is a logical 0, one stop bit is generated or checked in the data sent or received. If bit 2 is logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity-enable bit. When bit 3 is logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word

and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data-word bits and parity bit are summed.)

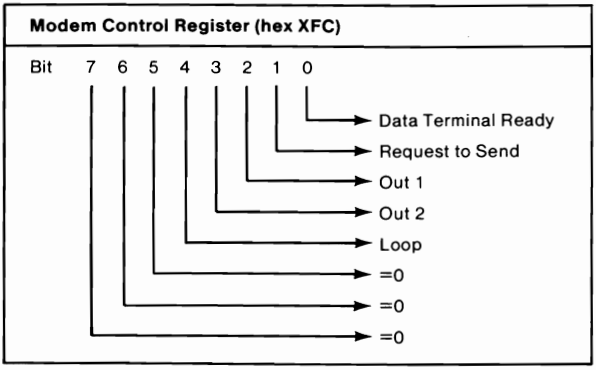
Bit 4 This bit is the even-parity-select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's are sent or checked in the data word bits and parity bit. When both bit 3 and bit 4 are a logical 1, an even number of bits are sent or checked.

Bit 5 This bit is the stuck-parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is sent and then detected by the receiver as a logical 0, if bit 4 is a logical 1, or as a logical 1 if bit 4 is a logical 0.

Bit 6 This bit is the set-break control bit. When bit 6 is set to a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set-break is disabled by setting bit 6 to logical 0. This feature enables the microprocessor to select a specific terminal in a computer communications system.

Bit 7 This bit is the divisor-latch access bit (DLAB). It must be set high (logical 1) to gain access to the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to gain access to the receiver buffer, the transmitter holding register, or the interrupt enable register.

Modem Control Register (hex XFC): This 8-bit register controls the data exchange with the modem or data set (an external device acting as a modem).



Modem Control Register

Bit 0 This bit controls the '-data terminal ready' (-DTR) output. When bit 0 is set to logical 1, the -DTR output is forced active. When bit 0 is reset to logical 0, the '-DTR' output is forced inactive.

Bit 1 This bit controls the '-request-to-send' (-RTS) output. Bit 1 affects the '-RTS' output in the same way bit 0 affects the '-DTR' output.

Bit 2 This bit controls the '-Output 1' (-OUT 1) signal, which is a spare the programmer can use. Bit 2 affects the '-OUT 1' output in the same way bit 0 affects the '-DTR' output.

Bit 3 This bit controls the '-Output 2' (-OUT 2) signal, which is a spare the programmer can use. Bit 3 affects the '-OUT 2' output in the same way bit 0 affects the '-DTR' output.

Bit 4 This bit provides a loopback feature for diagnostic testing of the controller. When bit 4 is set to logical 1, the following occur: the 'transmitter serial output' (SOUT) is set to the active state; the 'receiver serial input' (SIN) is disconnected; the output of the transmitter shift register is "looped back" to the receiver shift register input; the four modem-control inputs ('-CTS', '-DSR', '-RLSD', and '-RI') are

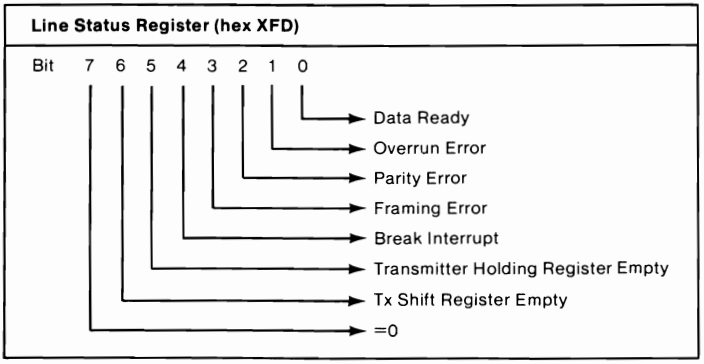
disconnected; and the four modem-control outputs ('-DTR', '-RTS', '-OUT 1' and '-OUT 2') are internally connected to the four modem control inputs. In the diagnostic mode, data sent is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the controller.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational, as are the modem-control interrupts. But the interrupts' sources are now the lower four bits of the modem control register (MCR) instead of the four modem-control inputs. The interrupts are still controlled by the interrupt enable register.

The controller's interrupt system can be tested by writing to the lower six bits of the line status register and the lower four bits of the modem status register. Setting any of these bits to logical 1 generates the appropriate interrupt (if enabled). Resetting these interrupts is the same as for normal controller operation. To return to normal operation, the registers must be reprogrammed for normal operation, and then bit 4 of the MCR must be reset to logical 0.

Bits 5–7 These bits are permanently set to logical 0.

Line Status Register (hex XFD): This 8-bit register provides the processor with status information about the data transfer.



Line Status Register

Bit 0 This bit is the receiver data ready (DR) indicator. It is set to logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to logical 0 by reading the data in the receiver buffer register.

Bit 1 This bit is the overrun error (OE) indicator. It indicates that data in the receiver's buffer register was not read by the processor before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator and indicates the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to logical 1 upon detection of a parity error, and is reset to logical 0 whenever the processor reads the contents of the line status register.

Bit 3 This bit is the framing error (FE) indicator. It indicates the received character did not have a valid stop bit. Bit 3 is set to logical 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level).

Bit 4 This bit is the break interrupt (BI) indicator. It is set to logical 1 whenever the received data input is held in the spacing state (logical 0) for longer than a full word transmission time (that is, the total time of start bit + data bits + parity bits + stop bits).

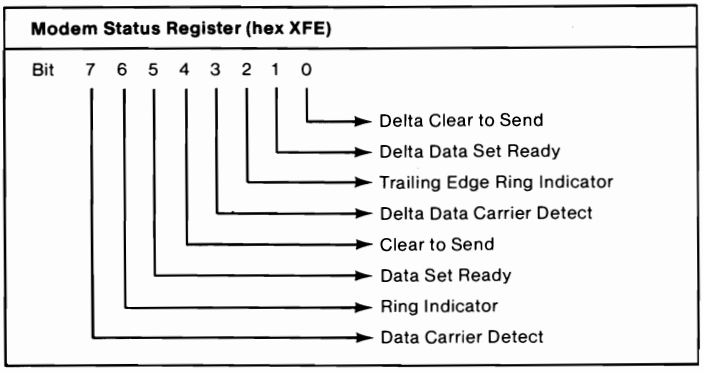
> **Note:** Bits 1 through 4 are error conditions that produce a receiver line-status interrupt whenever any of the corresponding conditions are detected.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. It indicates the controller is ready to accept a new character for transmission. In addition, this bit causes the controller to issue an interrupt to the processor when the THRE interrupt enable is set active. The THRE bit is set to logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. It is reset to logical 0 when the processor loads the transmitter holding register.

Bit 6 This bit is the transmitter empty (TEMT) indicator. It is set to logical 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to logical 0 if THR or TSR contain a data character.

Bit 7 This bit is permanently set to logical 0.

Modem Status Register (hex XFE): The 8-bit MSR provides the current state of the control lines from the modem (or external device) to the processor. In addition, four bits of the MSR provide change information. These four bits are set to logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the processor reads this register.



Modem Status Register

Bit 0 This bit is the delta clear-to-send (DCTS) indicator. It indicates the '-CTS' input to the chip has changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data-set-ready (DDSR) indicator. It indicates the '-DSR' input to the chip has changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing-edge ring-indicator (TERI) detector. It indicates the '-RI' input to the chip has changed from an active condition to an inactive condition.

Bit 3 This bit is the delta data-carrier-detect (DDCD) indicator. It indicates the '-DCD' input to the chip has changed state.

> **Note:** Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated.

Bit 4 This bit is the opposite of the '-clear-to-send' (-CTS) input. If bit 4 of the MCR loop is set to a logical 1, this bit is equivalent to RTS of the MCR.

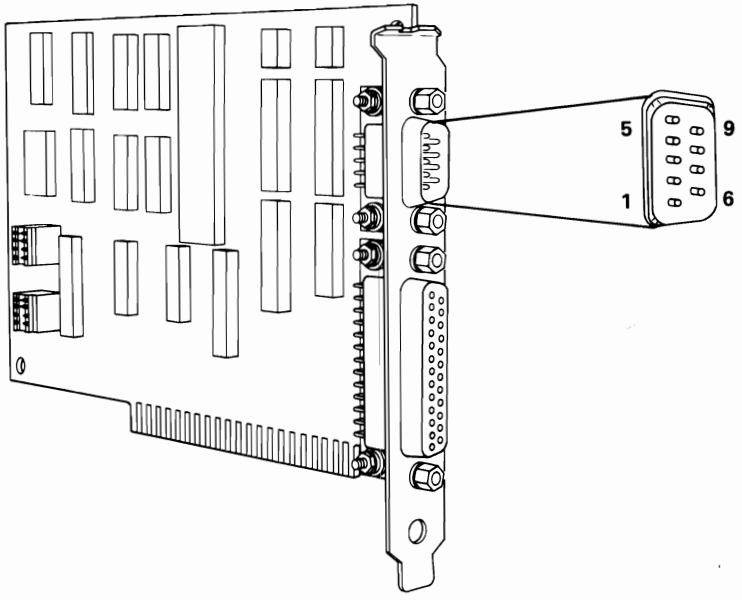
Bit 5 This bit is the opposite of the '-data-set-ready' (-DSR) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to DTR of the MCR.

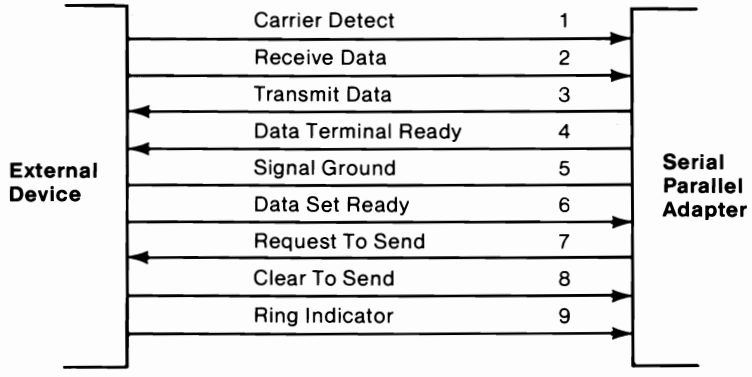
Bit 6 This bit is the opposite of the '-ring-indicator' (-RI) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 1 of the MCR.

Bit 7 This bit is the opposite of the '-data-carrier-detect' (-DCD) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 2 of the MCR.

Pin Assignment for Serial Port

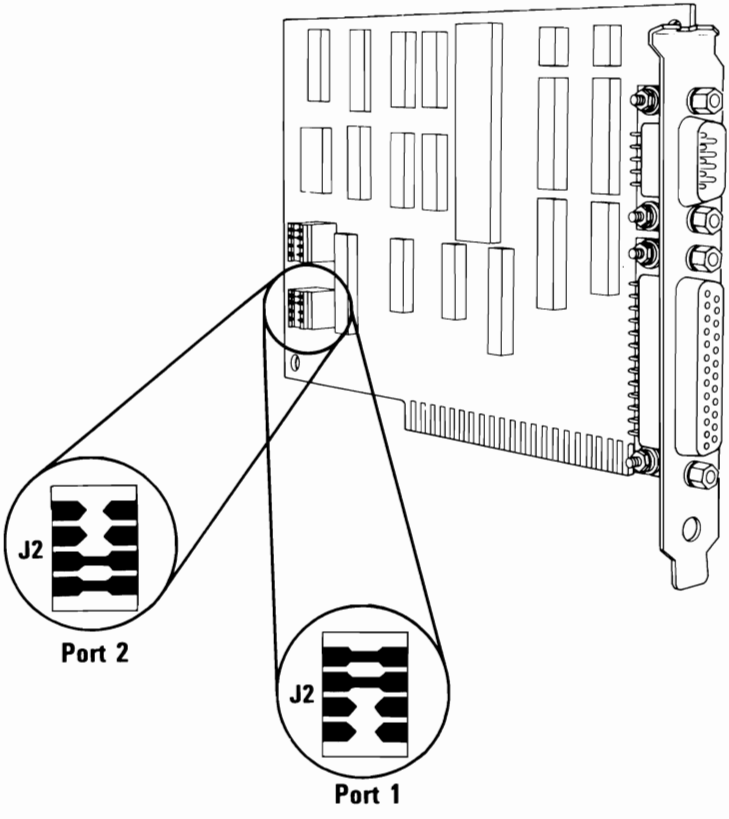
The following figure shows the pin assignments for the serial port in a communications environment.



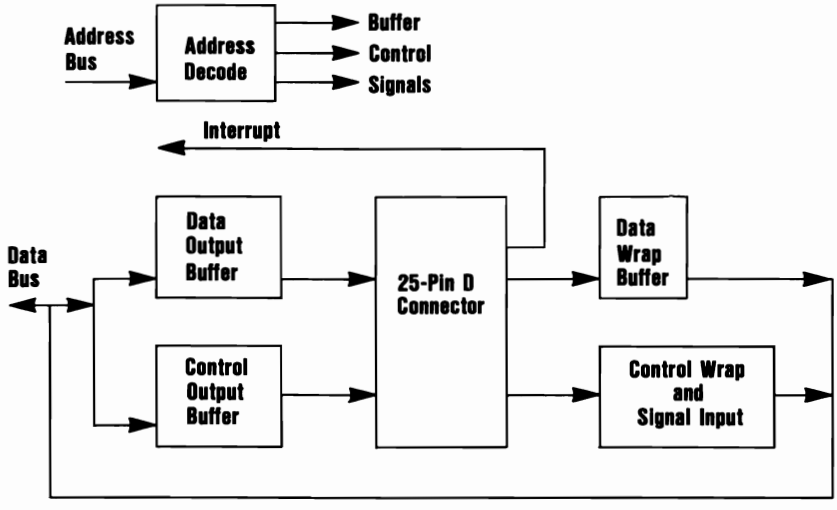


Parallel Portion of the Adapter

The parallel portion of the adapter makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL levels. The rear of the adapter has a 25-pin, D-shell connector. This port may be addressed as either parallel port 1 or 2. The port address is determined by the position of jumper J2, as shown in the following figure.



The following figure is a block diagram of the parallel portion of the adapter.



Parallel Portion Block Diagram

Printer Application

The following discusses the use of the parallel portion of the adapter to connect to a parallel printer. Hexadecimal addresses in this section begin with an X, which is replaced with a 3 to indicate port 1, or a 2 to indicate port 2.

Data Latch (hex X78, X7C)

Writing to this address causes data to be stored in the printer's data buffer. Reading this address sends the contents of the printer's data buffer to the system microprocessor.

Printer Controls (hex X7A, X7E)

Printer control signals are stored at this address to be read by the system microprocessor. The following are bit definitions for this byte.

Bit 7 Not used

Bit 6 Not used

Bit 5 Not used

Bit 4 +IRQ Enable—A logical 1 in this position allows an interrupt to occur when '-ACK' changes from active to inactive.

Bit 3 +SLCT IN—A logical 1 in this bit position selects the printer.

Bit 2 -INIT—A logical 0 starts the printer (50-microsecond pulse, minimum).

Bit 1 +AUTO FD XT—A logical 1 causes the printer to line-feed after a line is printed.

Bit 0 +STROBE—A 0.5-microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microsecond before and after the strobe pulse.

Printer Status - (hex X79, X7D)

Printer status is stored at this address to be read by the microprocessor. The following are bit definitions for this byte.

Bit 7 -BUSY—When this signal is active, the printer is busy and cannot accept data. It may become active during data entry, while the printer is offline, during printing, when the print head is changing positions, or while in an error state.

Bit 6 -ACK—This bit represents the current state of the printer's '-ACK' signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before '-BUSY' stops.

Bit 5 +PE—A logical 1 means the printer has detected the end of paper.

Bit 4 +SLCT—A logical 1 means the printer is selected.

Bit 3 -Error—A logical 0 means the printer has encountered an error condition.

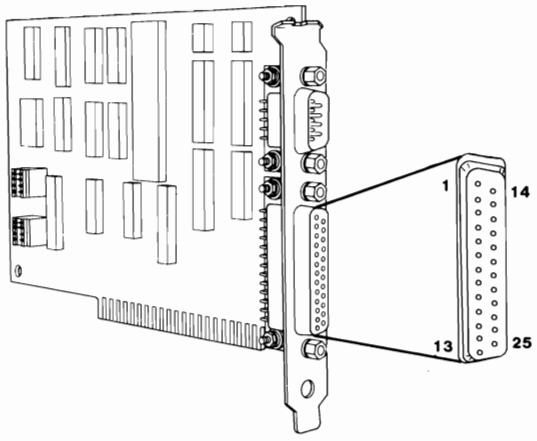
Bit 2 Unused.

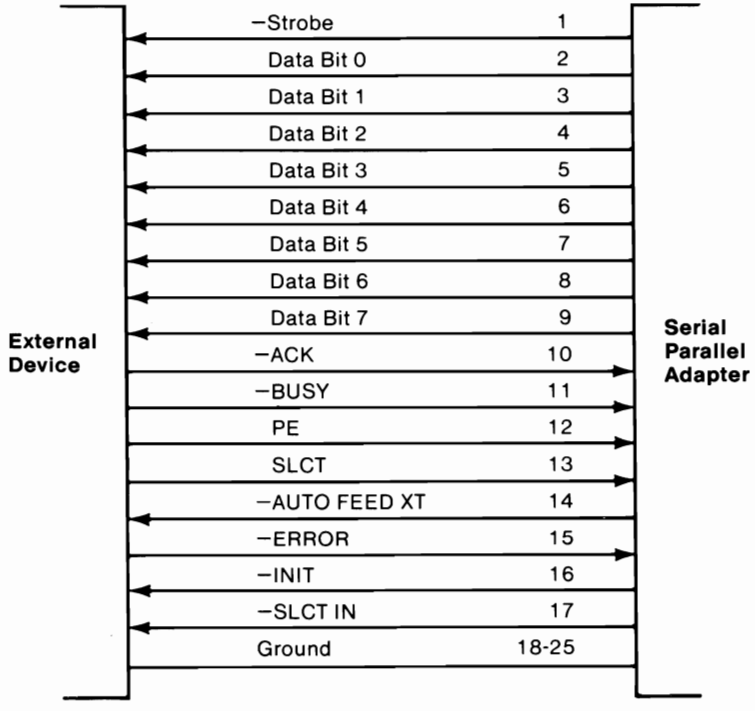
Bit 1 Unused.

Bit 0 Unused.

Parallel Interface

The adapter has a 25-pin, D-shell connector at the rear of the adapter. The following figure shows the signals and their pin assignments. Typical printer input signals also are shown.





Specifications

The following figures list characteristics of the output driver.

Sink current	24 mA	Max
Source Current	-2.6 mA	Max
High-Level Output Voltage	2.4 Vdc	Min
Low-Level Output Voltage	0.5 Vdc	Max

Parallel Data and Processor IRQ

Sink Current	16 mA	Max
Source Current	0.55 mA	Max
High Level Output Voltage	5 Vdc	Minus Pull-Up
Low Level Output Voltage	0.4 Vdc	Max

Parallel Control

Sink Current	24 mA	Max
Source Current	-15 mA	Max
High Level Output Voltage	2.0 Vdc	Min
Low Level Output Voltage	0.5 Vdc	Max

Parallel Processor Interface (Except IRQ)

The following are the specifications for the serial interface.

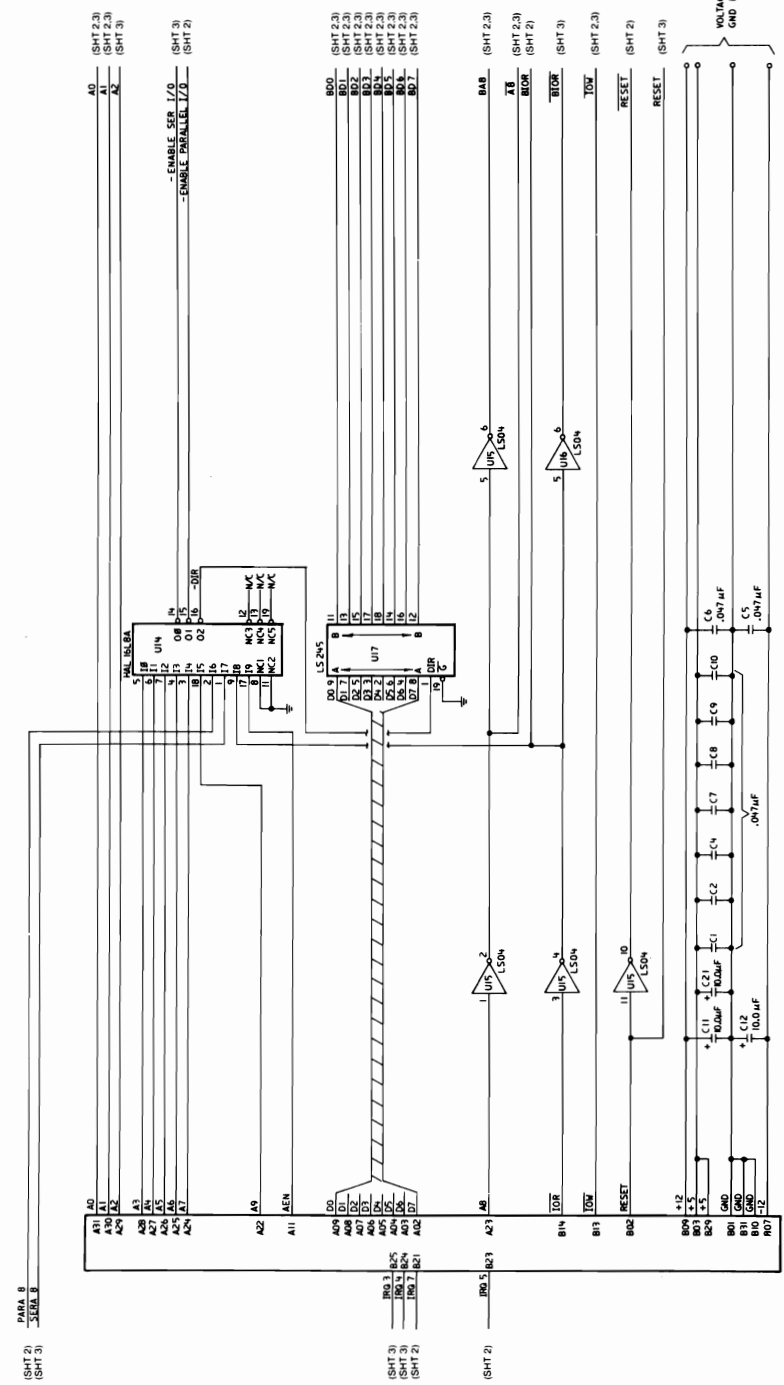
Function	Condition
On	Spacing condition (binary 0, positive voltage).
Off	Marking condition (binary 1, negative voltage).

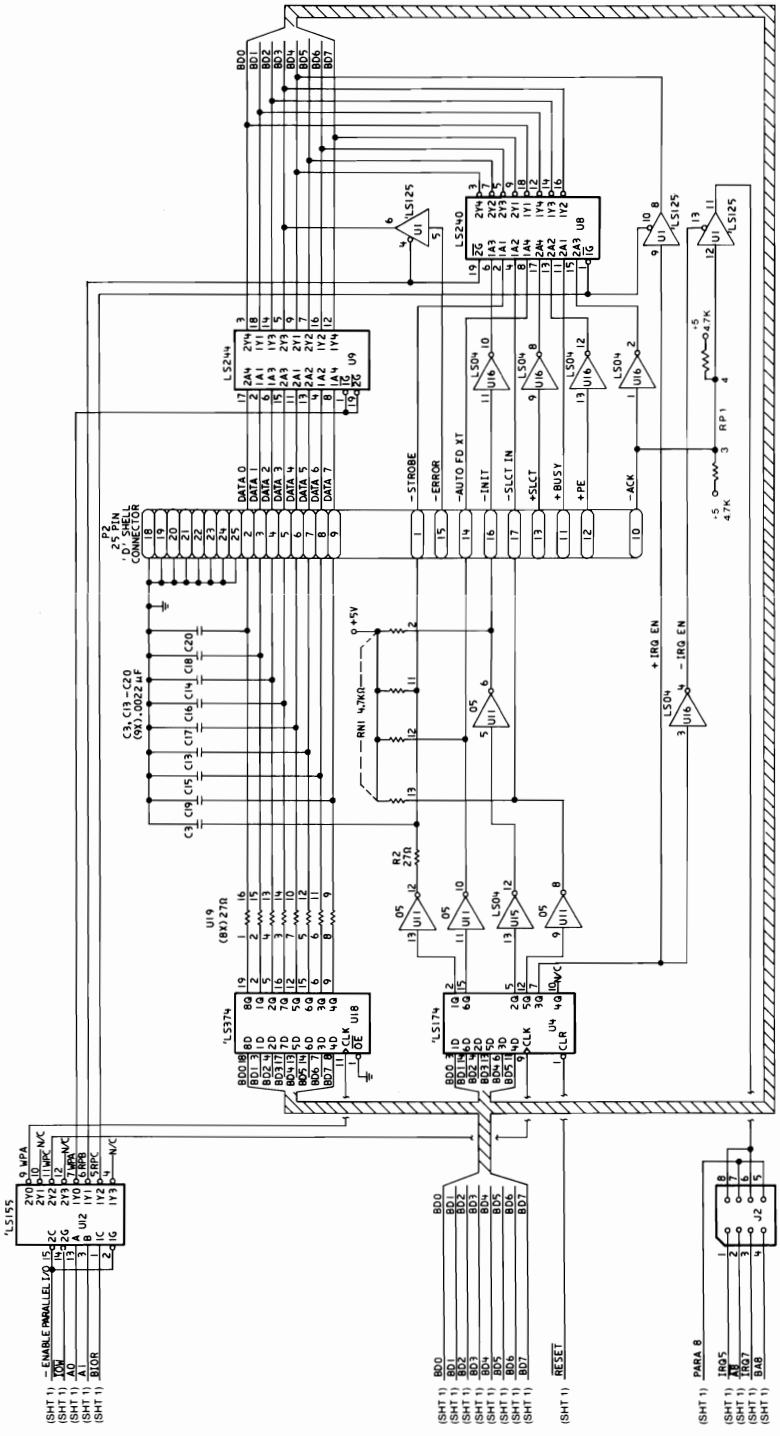
Voltage	Function
Above +15 Vdc	Invalid
+3 Vdc to +15 Vdc	On
-3 Vdc to +3 Vdc	Invalid
-3 Vdc to -15 Vdc	Off
Below -15 Vdc	Invalid

Serial Port Functions

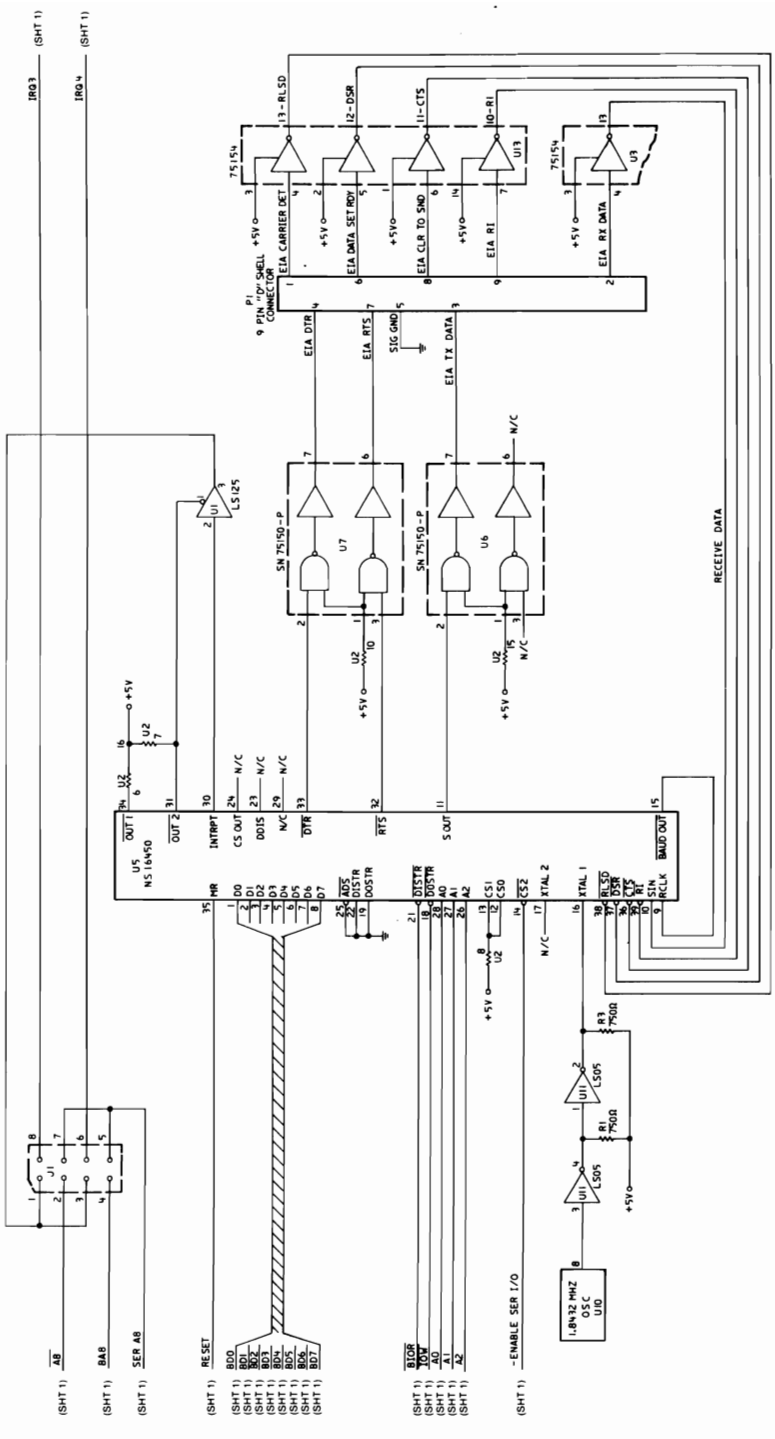
Notes:

Logic Diagrams





August 31, 1984



Serial/Printer Adapter (Sheet 3 of 3)

Notes: