Personal Computer Hardware Reference Library

Prototype Adapter

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Description

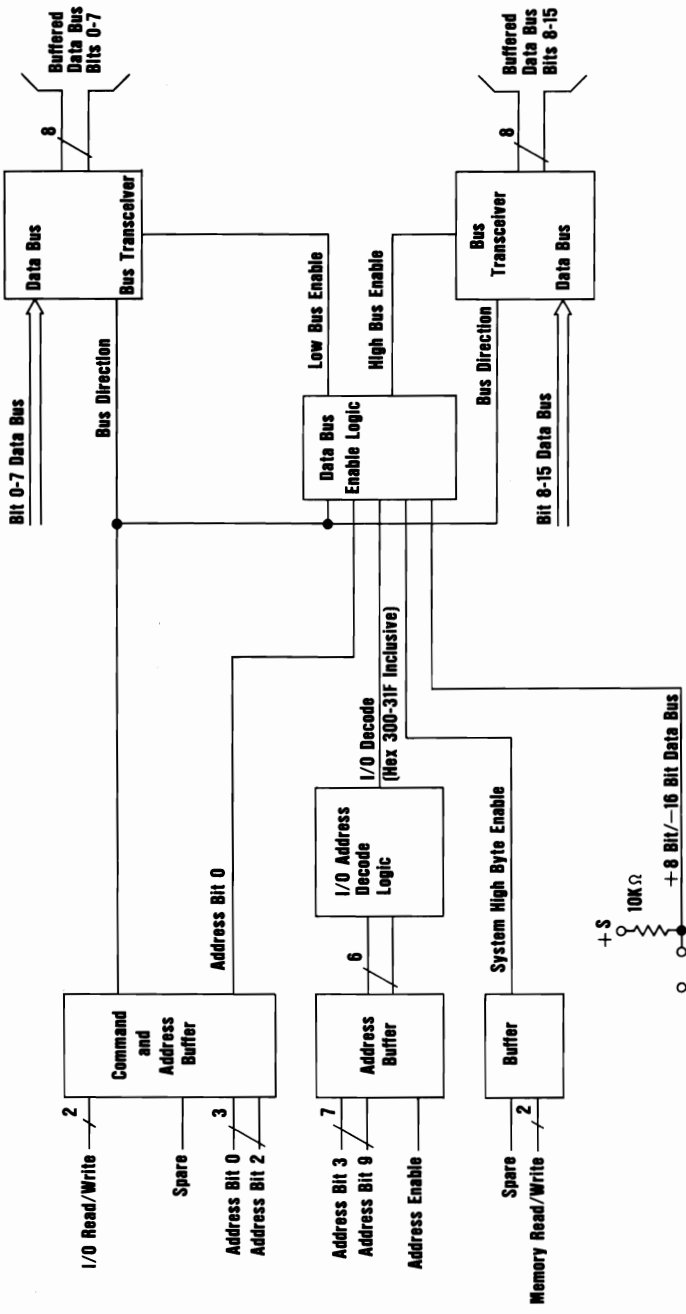
The IBM Personal Computer AT Prototype Adapter is 121.9 millimeters (4.8 inches) high by 333.25 millimeters (13.12 inches) long and plugs into any system-unit expansion slot except number 1 or 7. Two card-edge tabs, one 2- by 31-position and one 2- by 18-position, provide all system control signals and voltages.

The adapter has a voltage bus (+5 Vdc) and a ground bus (0 Vdc). Each bus borders the adapter, with the ground bus on the component side and the voltage bus on the pin side. A system interface is also provided on the adapter with a jumper to specify whether the device has an 8- or a 16-bit data bus.

This adapter also accommodates a D-shell connector from 9 to 37 positions.

> **Note:** All components must be installed on the component side of the adapter. The total width of the adapter, including components, may not exceed 12.7 millimeters (0.5 inch). If these specifications are not met, components on the IBM Personal Computer AT Prototype Adapter may touch other adapters plugged into adjacent expansion slots.

The following is a block diagram of the IBM Personal Computer AT Prototype Adapter.



Prototype Adapter Block Diagram

Adapter Design

The following information is provided to assist in designing an adapter using the IBM Personal Computer AT Prototype Adapter.

Designing an Input/Output Adapter

The following information may be used to design an input/output type of adapter.

Programming

Insert a Jump instruction after all I/O read (IOR) or I/O write (IOW) assembler language instructions to avoid a potential timing problem caused by slow I/O devices. The following figure shows a typical programming sequence.

Before	After	
Your Code		Your Code
IOR		IOR
Your Code		JMP NEXT
	NEXT:	Your Code

Program Sequence

Jumper Wire (J1)

Your design can use either 8 bits of the data bus (jumper off) or the full 16 bits of the data bus (jumper on). Most devices have 8-bit data buses.

Wait-State Generator Circuits

If your device runs too slow, you must add a wait-state generator to make the I/O read and write signals longer. First, determine the time needed by your device from the start of an IOR signal until it can put data on the system's data bus. Next, compare that

time with the time given by the system's microprocessor. The system microprocessor gives 750 nanoseconds for 8-bit devices and 250 nanoseconds for 16-bit devices.

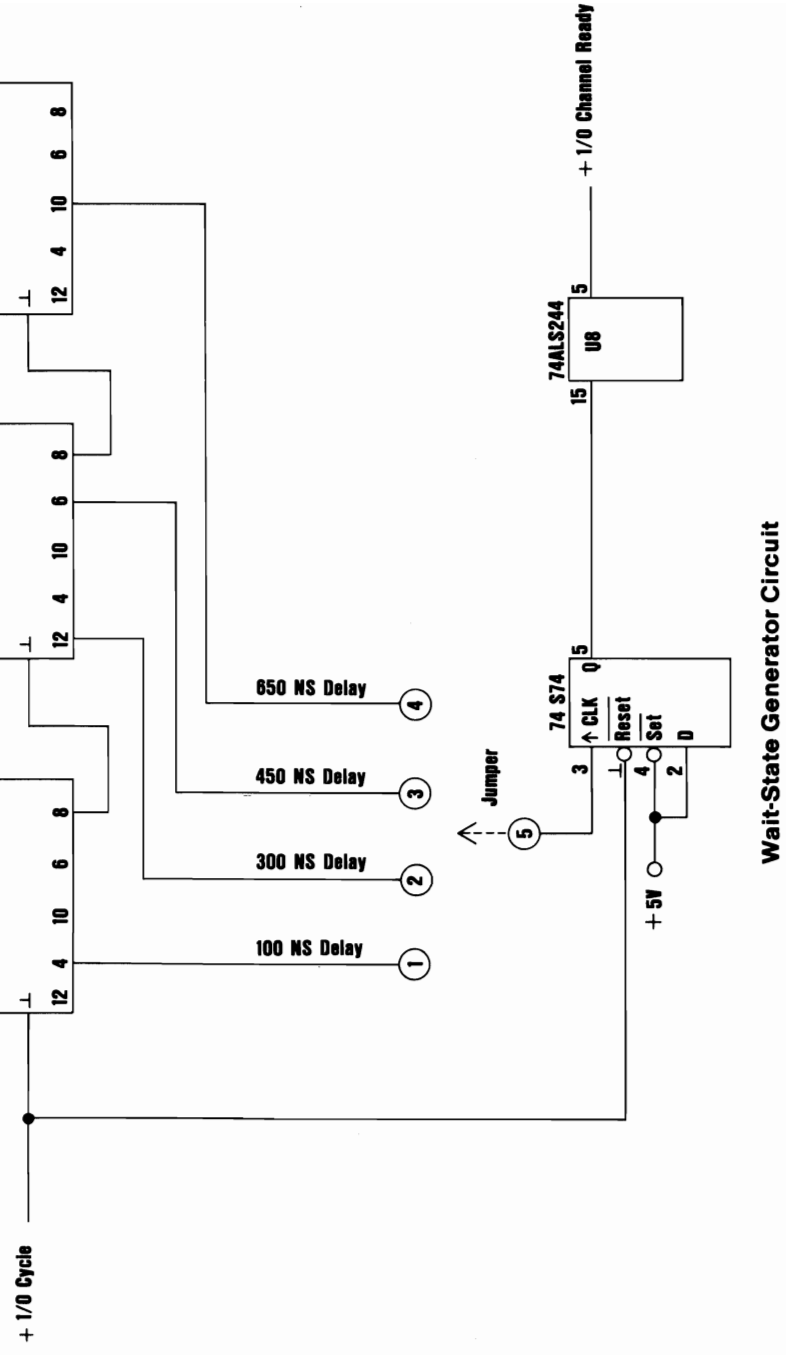
A similar problem may exist for an IOW signal. Determine the write data setup time, which is the time required by your design from the time it is given valid data until it is told to take this data by the IOW signal. The time given by the system microprocessor from when data is first valid to the device until the IOW signal goes active and then inactive is shown in the following figure. Your design can take the data when IOW goes active (less setup time) or when IOW goes inactive (more setup time).

8-Bit Device	16-Bit Device	Description
100 ns	100 ns	Data Valid Until IOW is Active.
850 ns	350 ns	Data Valid Until IOW is Inactive.

IOW Timing

If the time given by the system microprocessor is not enough, you must add a wait-state generator circuit that will provide longer IOR and IOW signals. A recommended wait-state generator circuit is shown in the following figure.

> **Note:** Pulse Engineering Inc. PE21214 is the delay module used.



Wait-State Generator Circuit

Note: To add wait states and increase the time given by the microprocessor for I/O Read and Write commands, install one of the following jumpers.

- 16-Bit Design

  1 wait state 250 nanoseconds--No jumper

  2 wait states 417 nanoseconds--Jumper 1 to 5

  3 wait states 583 nanoseconds--Jumper 2 to 5

  4 wait states 750 nanoseconds--Jumper 3 to 5

  5 wait states 917 nanoseconds--Jumper 4 to 5

- 8-Bit Design

  4 wait states 750 nanoseconds--No Jumper

  5 wait states 917 nanoseconds--Jumper 4 to 5

Designing a Memory Adapter

The following information may be used to design a memory adapter.

Control Lines

There are two sets of memory control lines. '-SMEMR' for system-memory read, and '-SMEMW' for system-memory write. They are active when accessing memory in the first megabyte (address bits 20 through 23 are all off). If you use these lines, you can avoid an address decode circuit that checks for address bits 20 through 23 being off.

The other set of control lines is '-MEMR' and '-MEMW'. These are active when addressing all memory locations. If you wish to design memory that will answer to addresses above the

first megabyte, you must use these lines and decode address bits 20 through 23 to select the particular address range your memory occupies.

System Address Lines (SA)

The 20 lowest-order address lines are 'SA0' through 'SA19'. SA address bits are active a minimum of 30 nanoseconds before a control line goes active, and they stay active a minimum of 66 nanoseconds *after* the control line goes inactive. Timings are at the adapter socket.

Local Address Lines (LA)

There are seven high-order address lines called 'LA17' through 'LA23'. LA address bits are active a minimum of 159 nanoseconds before a control line goes active, and they typically stay active 83 nanoseconds *before* the control line goes inactive. LA bits should be decoded to select the particular address range your memory occupies. Because this decode will go inactive 83 nanoseconds before the control line goes inactive, it may be necessary to latch the decode. The output of this decoder circuit should be connected to the input of a transparent latch, such as a 74ALS573 (+BALE should be connected to the clock pin on the latch). If this is done, the output of the 74LS573 will be active approximately 30 nanoseconds before a control line goes active, and will stay active approximately 66 nanoseconds *after* the control line goes inactive. Timings are at the adapter socket.

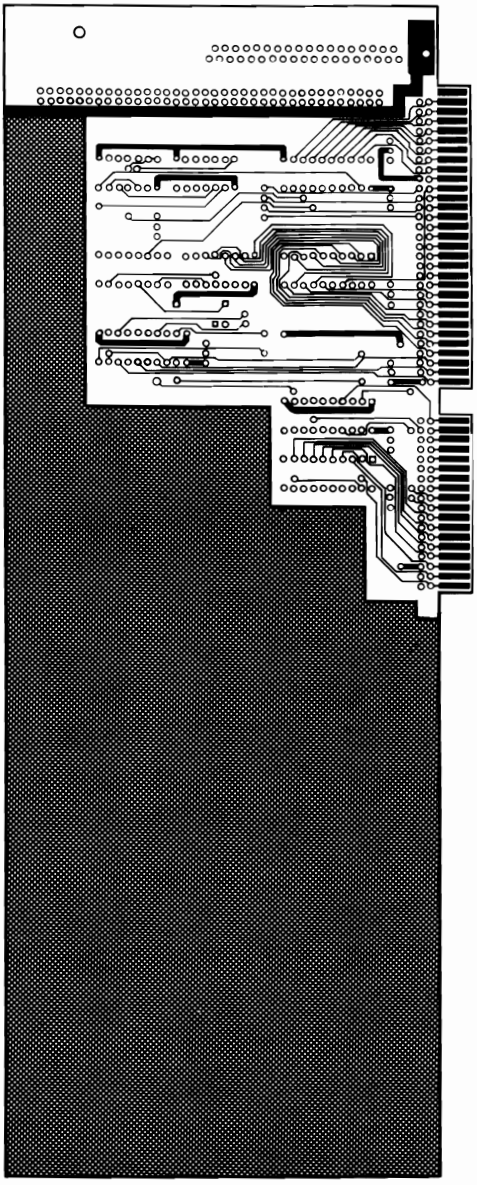
IBM Personal Computer AT Prototype Adapter Layout

The IBM Personal Computer AT Prototype Adapter has two layers screened onto it: one on the front and one on the back. It also has 4,311 plated through-holes that are 10.1 millimeters (0.04 inch) wide and have a 1.52-millimeter (0.06-inch) pad. These holes are arranged in a 2.54-millimeter (0.1-inch) grid. There are 37 plated through-holes, 1.22 millimeters (0.048 inch) wide, on the rear of the adapter that are used for a 9- to 37-position D-shell connector. The adapter also has 5 holes that

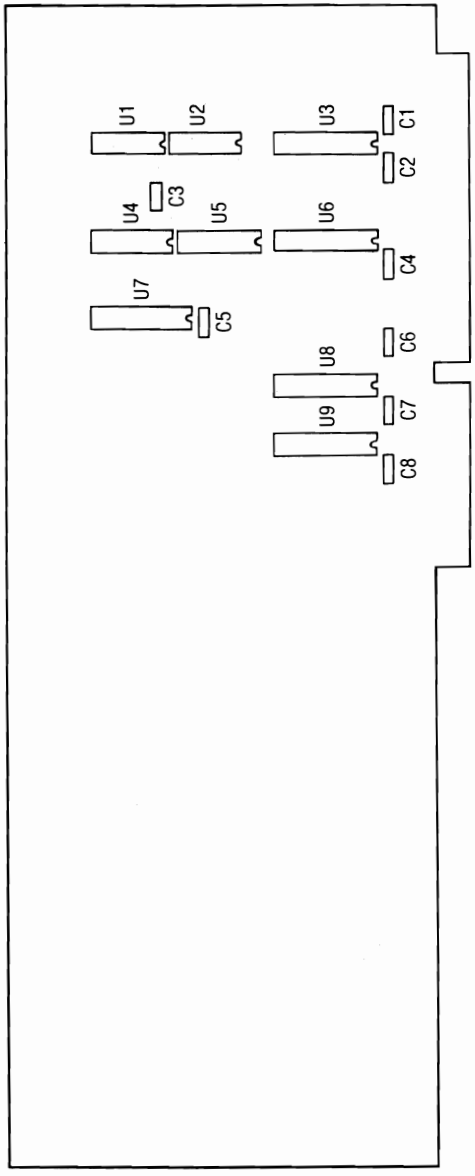
are 3.18 millimeters (0.125 inch) wide. One of these is just above the two rows of D-shell connector holes, and each of the other four is in a corner of the adapter.

Component Side

The component side of the adapter has a ground bus, 1.27 millimeters (0.05 inch) wide screened onto it and two card-edge tabs labeled A1 through A31 and C1 through C31. The following figure shows the ground bus and card edge-tabs.

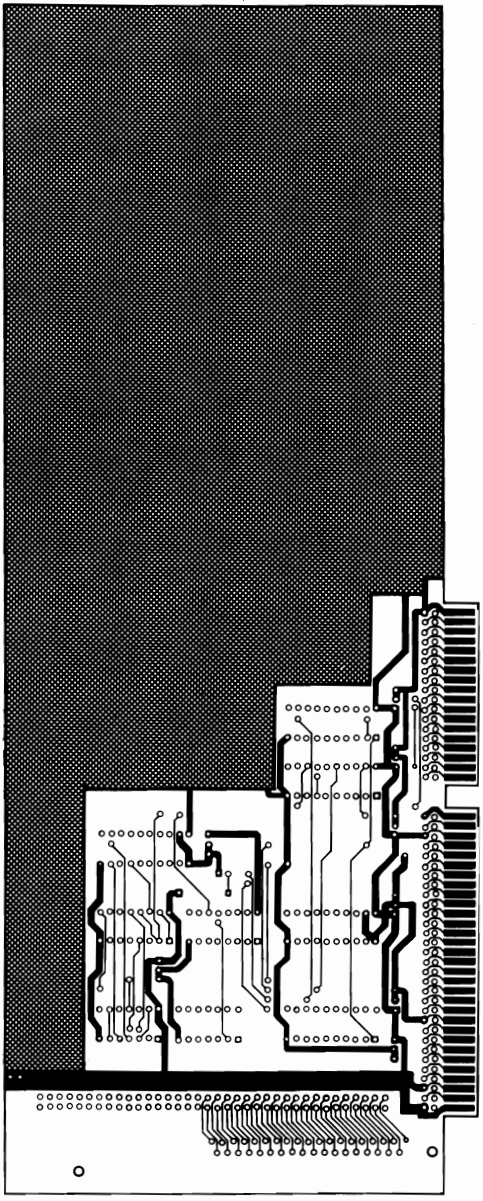


The component side of the adapter also has a silk screen printed on it that may be used as a component guide for the I/O interface. The following figure shows this silk screen.



Pin Side

The pin side of the adapter has a 5-Vdc bus, 1.27 millimeters (0.05 inch) wide, screened onto it, and two card-edge tabs: labeled B1 through B31 and D1 through D18. The following figure shows the 5-Vdc bus and card edge-tabs.



Card-Edge Tabs

Each card-edge tab is connected to a plated through-hole by a 0.3-millimeter (0.012-inch) land. Four ground tabs are connected to the ground bus by four 0.3-millimeter (0.012-inch) lands, and three 5 Vdc tabs are connected to the 5-Vdc bus by three 0.3-millimeter (0.012 inch) lands.

Additional Information

Additional information regarding the I/O interface may be found under 'I/O Channel' in Section 1 of IBM Personal Computer AT *Technical Reference* manual. Logic diagrams of the IBM Personal Computer AT Prototype Adapter may be found later in this section. If the recommended interface logic is to be used, the following figure shows the recommended components and their TTL numbers.

Component	TTL #	Description
U1	74S00	Quad 2 Input NAND
U2	74S10	Triple 3 Input NAND
U3, U9	74LS245	Octal Bus Transceiver
U4	74S139	Dual 1 of 4 Decoder
U5	74S138	1 of 8 Decoder
U6, U7, U8	74ALS244	Octal Buffers
C1, C6		10-Microfarad Tantalum Capacitor
C2, C3, C4, C5, C7, C8		0.047-Microfarad Ceramic Capacitor
R1		10 Kohm, .25-Watt, 10% Resistor (Axial Leads)
J1		Jumper Wire

Recommended Components

Note: J1, U8, and U9 are not required for a design using only the low-order 8 bits of the data bus. Designs using all 16 bits of the data bus require these components.

Interfaces

Internal Interface

Because of the number of adapters that may be installed in the system, I/O bus loading should be limited to 1 Schottky TTL load. If the recommended interface logic is used, this requirement is met. Power limitations may be found under 'Power Supply' in the IBM Personal Computer AT *Technical Reference* Manual.

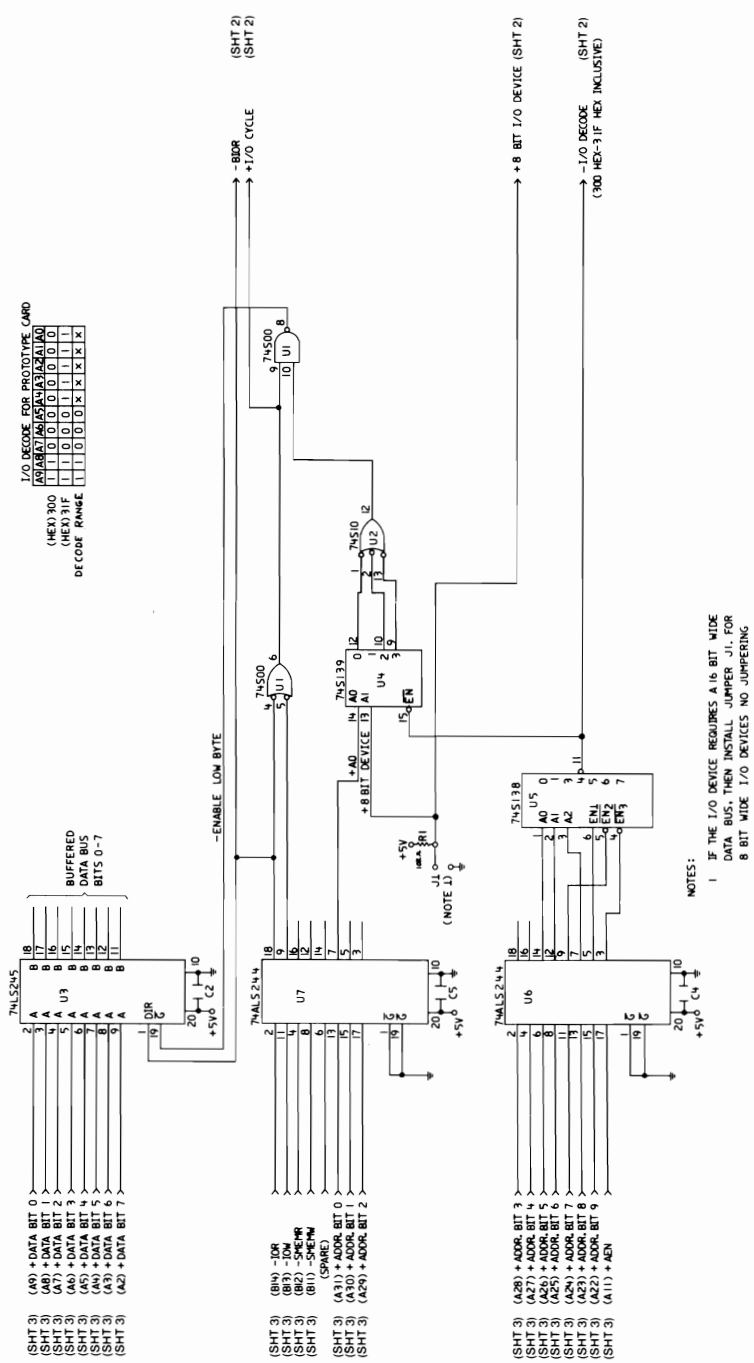
External Interface

The following figure lists the recommended connectors for the rear of the adapter.

Connector	Part no. (Amp) or Equivalent
9-Pin D-Shell (Male)	205865-1
9-Pin D-Shell (Female)	205866-1
15-Pin D-Shell (Male)	205867-1
15-Pin D-Shell (Female)	205868-1
25-Pin D-Shell (Male)	205857-1
25-Pin D-Shell (Female)	205858-1
37-Pin D-Shell (Male)	205859-1
37-Pin D-Shell (Female)	205860-1

Recommended Connectors

Logic Diagrams



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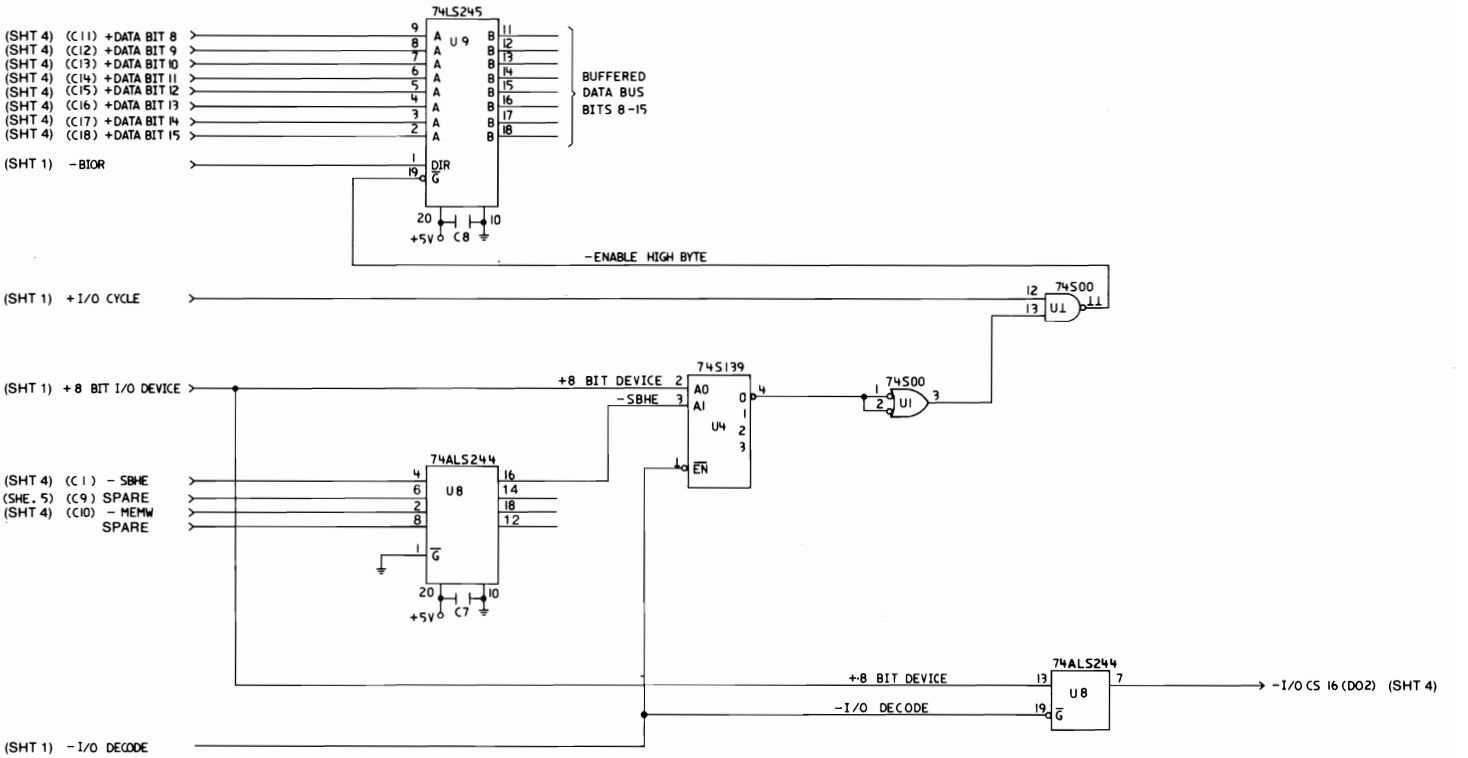

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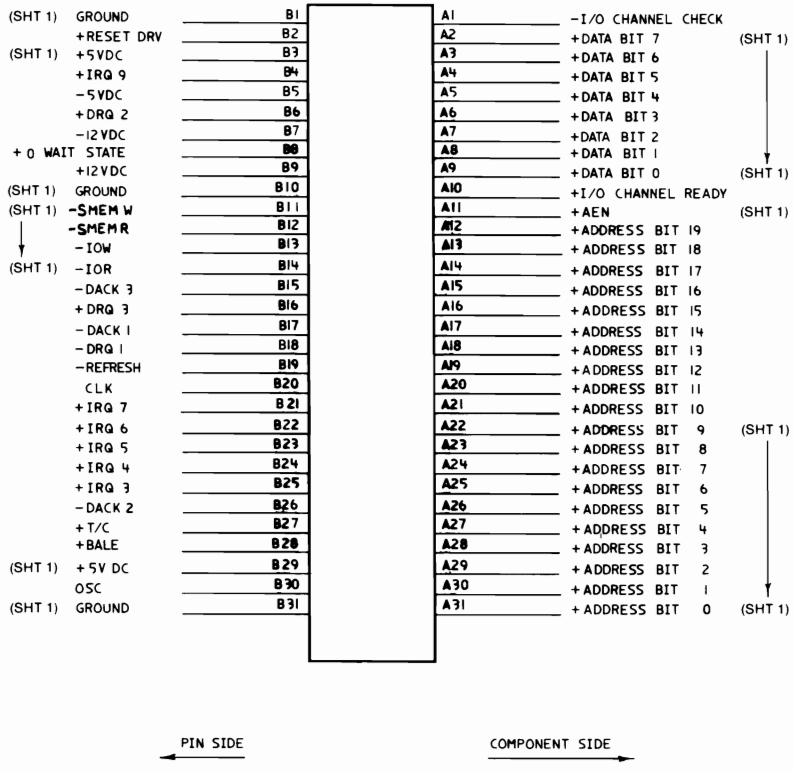

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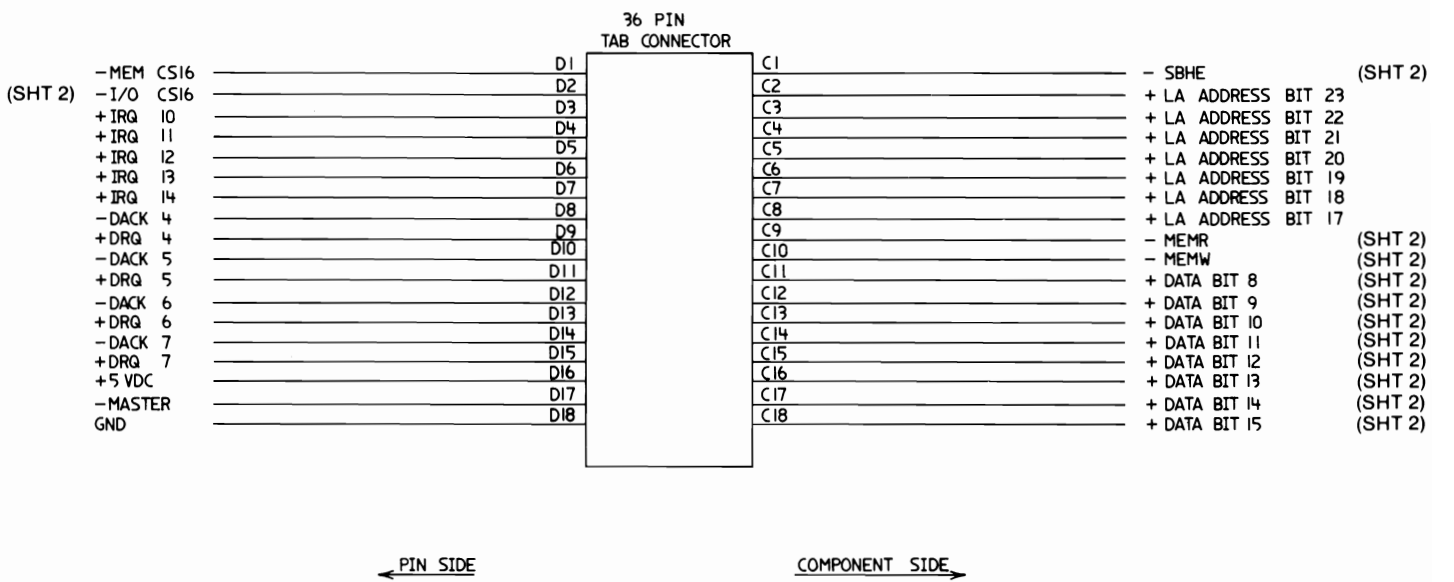

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Notes: