MOS LSI

TMS 4132 JDL
32,768-BIT DYNAMIC RANDOM-ACCESS MEMORY

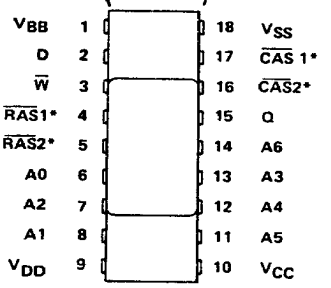
NOVEMBER 1978

- 32,768 × 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL-Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE CYCLE (MIN)
TMS 4132-15	150 ns	100 ns	375 ns	375 ns
TMS 4132-20	200 ns	135 ns	375 ns	375 ns
TMS 4132-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - — Operating . . . 380 mW (typ)
  - — Standby . . . 18 mW (typ)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- Dual 18-Pin 300-Mil (7.62 mm) Package Configuration

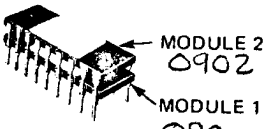
18-PIN SIDEBRAZE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



ZAC900

* Module 1: RAS1 and CAS1 apply, Pins 5 and 16 are No-Connects
Module 2: RAS2 and CAS2 apply, Pins 4 and 17 are No-Connects.

(ANGULAR VIEW)



PIN NOMENCLATURE			
A0-A6	Address Inputs	W	Write Enable
CAS1	Column address strobe, Module 1	VBB	5-V power supply
CAS2	Column address strobe, Module 2	VCC	+5-V power supply
D	Data input	VDD	+12-V power supply
Q	Data output	VSS	0 V ground
RAS1	Row address strobe, Module 1		
RAS2	Row address strobe, Module 2		

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004307
4307 TJ

description

The TMS 4132 consists of two TMS 4116 16,384 bit high speed MOS dynamic random access memories, each in its own package. The two packages are permanently connected, pin for pin, one on top of the other. The lower TMS 4116 is referred to as Module 1, the upper TMS 4116 as Module 2. The result is a 18-pin memory device organized as 32,768 words of one bit each with essentially the same characterstics of the TMS 4116, NMOS single-transistor cell dynamic RAM.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobes, RAS1 and RAS2, and Column Address Strobes, CAS1 and CAS2. All address lines (A0 through A6) and data-in (D) are latched on-chip to simplify system design. Data-out (Q) is unlatched to allow greater system flexibility.

PRELIMINARY DATA SHEET: Supplementary data will be published at a later date.

Typical power dissipation, for both modules, at any given time is less than 380 milliwatts active, 20 milliwatts standby (V_{CC} is not required during standby operation). To retain the data (both modules) only the standby power of 18 milliwatts is required which includes the power consumed to refresh the contents of the memory.

The TMS 4132 JDL is offered in a stacked 18-pin dual-in-line sidebraze package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers.

operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of the 16,384 storage cell locations on each module. To address a storage location on module 1 seven row address bits are set up on pins A0 through A6 and latched onto the chip by row-address-strobe 1 ($\overline{RAS}1$). Then the seven column address bits are set up on the same pins and are latched onto the chip by column-address-strobe 1 ($\overline{CAS}1$). To address a storage location on module 2 the same procedure is followed, however addresses are now strobed in using row-address-strobe 2 ($\overline{RAS}2$) and column address strobe 2 ($\overline{CAS}2$). When $\overline{RAS}1$ and $\overline{CAS}1$ are being used (i.e. Module 1 selected), $\overline{RAS}2$ and $\overline{CAS}2$ should be high (and vice-versa of Module 2 is selected). All addresses must be stable on or before the falling edges of $\overline{RAS}1$ (or $\overline{RAS}2$) and $\overline{CAS}1$ (or $\overline{CAS}2$). Each $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder of the module. Each $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers of the module. The device whose $\overline{RAS}$ and $\overline{CAS}$ are high are put into a standby mode.

write enable ($\overline{W}$)

For either module, the read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

For either module, data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brough low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

For either module a three state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

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refresh

A refresh operation must be performed at least every two milliseconds on both modules. Since the output buffer is in the high impedance state unless $\overline{CAS}1$ (or $\overline{CAS}2$) is applied, a $\overline{RAS}$ only refresh sequence avoids any output during refresh. Both $\overline{RAS}$ 1 and $\overline{RAS}2$ should strobe each of the 128 row addresses on each module simultaneously in order to refresh each bit in each row. $\overline{CAS}1$ and $\overline{CAS}2$ can remain high (inactive) for the refresh sequence to conserve power.

page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond all column locations on a single TMS 4132, the row address and $\overline{RAS}1$ or $\overline{RAS}2$ is applied to multiple 16K or 32K RAMs and $\overline{CAS}1$ or $\overline{CAS}2$ is decoded to select the proper RAM.

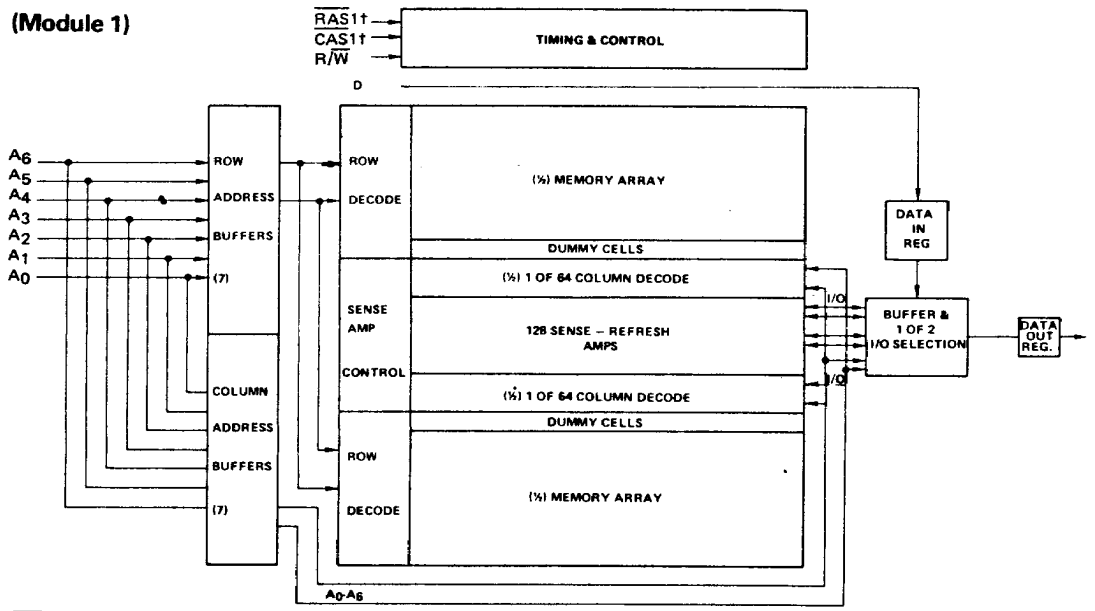
power-up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

TMS 4132 JDL
32,768-BIT DYNAMIC RANDOM-ACCESS MEMORY

functional block diagram

(Module 1)



†$\overline{RAS2}$ and $\overline{CAS2}$ if Module 2 is selected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin (see Note 1)	−0.5 to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS}	−1 to 15 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{DD}	10.8	12	13.2	V
Supply voltage, V_{SS}		0		V

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA (one module selected)	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA (one module selected)			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V (both modules selected)	−20		20	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}1$ and $\overline{CAS}2$ high (both modules selected)	−20		20	μA
I_{BB1}	Average operating current during read or write cycle	Minimum cycle time (one module selected)		110	300	μA
I_{CC1}*					4 **	mA
I_{DD1}				30	TBD	mA
I_{BB2}	Standby current	After 1 memory cycle $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ high (both modules deselected)		20	200	μA
I_{CC2}				−20	20	μA
I_{DD2}				1.5	TBD	mA
I_{BB3}	Average refresh current	Minimum cycle time $\overline{RAS}1$ and $\overline{RAS}2$ cycling, $\overline{CAS}1$ and $\overline{CAS}2$ high (both modules selected)		200	400	μA
I_{CC3}			−20		20	μA
I_{DD3}				40	54	mA
I_{BB4}	Average page-mode current	Minimum cycle time $\overline{RAS}1$ or $\overline{RAS}2$ low, $\overline{CAS}1$ or $\overline{CAS}2$ cycling (one module selected)		60	300	μA
I_{CC4}*					4 **	
I_{DD4}				20.5	28.5	mA

*V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.
**Output loading two standard TTL loads.
TBD indicates parameter is To Be Determined.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	8	10	pF
$C_{i(D)}$	Input capacitance, data input	8	10	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	16	20	pF
$C_{i(W)}$	Input capacitance, write enable input	16	20	pF
C_o	Output capacitance	10	14	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS 4132-15		TMS 4132-20		TMS 4132-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from row address strobe	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		150		200		250	ns
t_{PXZ}	Output disable time	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS 4132-15		TMS 4132-20		TMS 4132-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	170		225		275		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(RW)}$	Read, modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse width, column address strobe high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse width, column address strobe low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse width, row address strobe high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse width, row address strobe low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		75		ns
t_T	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	35	3	50	3	50	ns
$t_{su(AC)}$	Column address setup time	t_{ASC}	−10		−10		−10		ns
$t_{su(AR)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(ACL)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(AR)}$	Row address hold time	t_{RAH}	20		25		35		ns
$t_{h(ARL)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(CRL)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	150		200		250		ns
$t_{h(DCL)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		75		ns
$t_{h(DRL)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(DWL)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		75		ns
$t_{h(rd)}$	Read command hold time	t_{RCH}	0		0		0		ns
$t_{h(WCL)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(WRL)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{CHRL}	Delay time, column address strobe high to row address strobe	t_{CRP}	−20		−20		−20		ns
t_{CLRH}	Delay time, column address strobe low to row address strobe high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, column address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{CWD}	70		95		125		ns
t_{REF}	Refresh period	t_{REF}		2		2		2	ms
t_{RLCL}	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, row address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, $\overline{W}$ low to column address strobe low (early write cycle)	t_{WCS}	−20		−20		−20		ns

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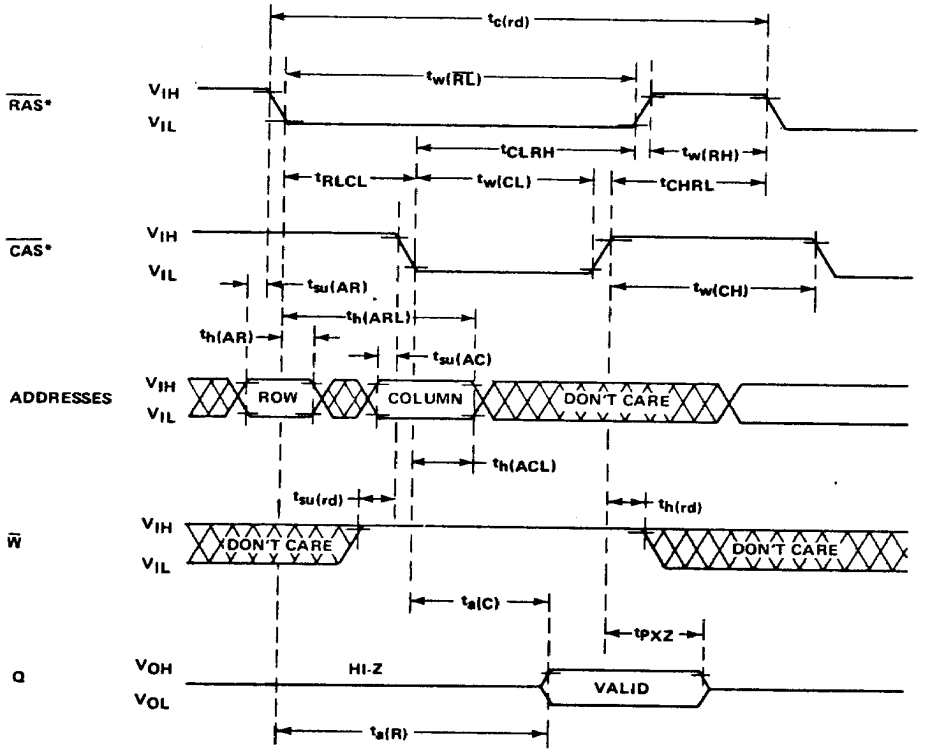
free-air temperature

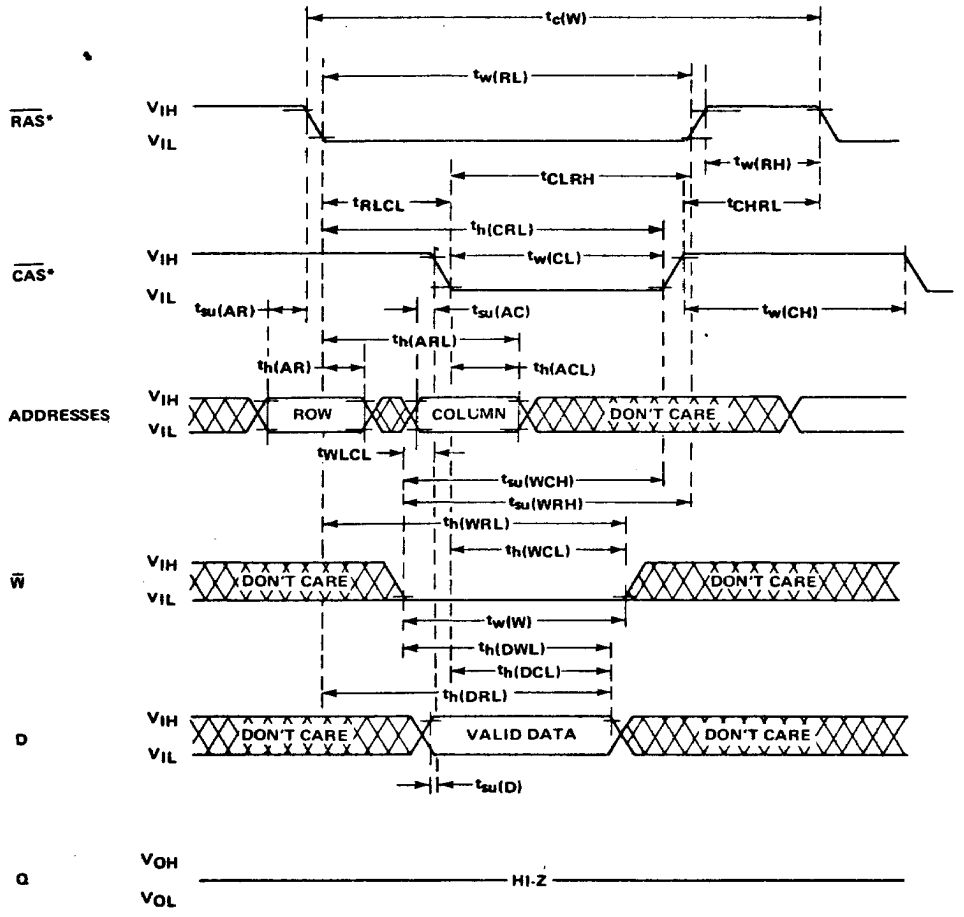
4132-20	TMS 4132-25		UNIT
MAX	MIN	MAX	
	275		ns
	410		ns
	410		ns
	515		ns
	100		ns
10,000	165	10,000	ns
	150		ns
10,000	250	10,000	ns
	75		ns
50	3	50	ns
	−10		ns
	0		ns
	0		ns
	0		ns
	100		ns
	100		ns
	75		ns
	35		ns
	160		ns
	250		ns
	75		ns
	160		ns
	75		ns
	0		ns
	75		ns
	160		ns
	−20		ns
	165		ns
	125		ns
2		2	ms
65	35	85	ns
	200		ns
	−20		ns

read cycle timing



*If module 1 is selected these are $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ remain high.
If module 2 is selected these are $\overline{RAS}2$ and $\overline{CAS}2$, $\overline{RAS}1$ and $\overline{CAS}1$ remain high.

early write cycle timing



*If module 1 is selected these are $\overline{RAS}$1 and $\overline{CAS}$1, $\overline{RAS}$2 and $\overline{CAS}$2 remain high.
If module 2 is selected these are $\overline{RAS}$2 and $\overline{CAS}$2, $\overline{RAS}$1 and $\overline{CAS}$1 remain high.

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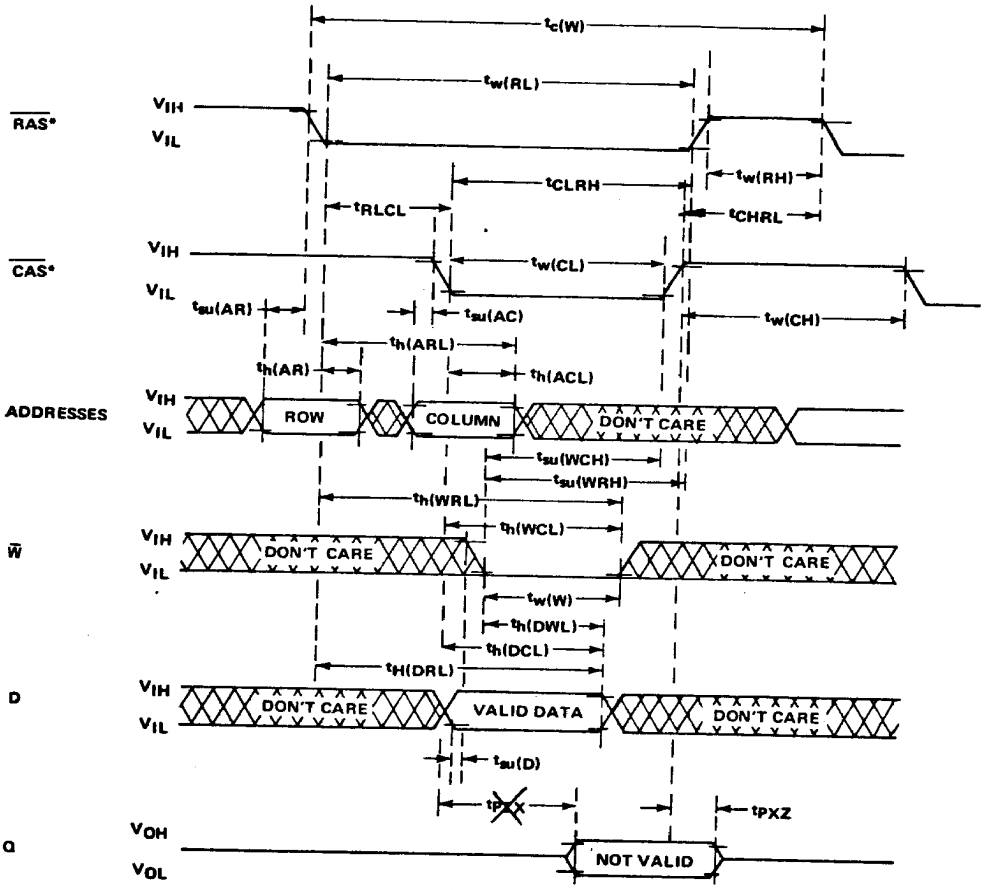
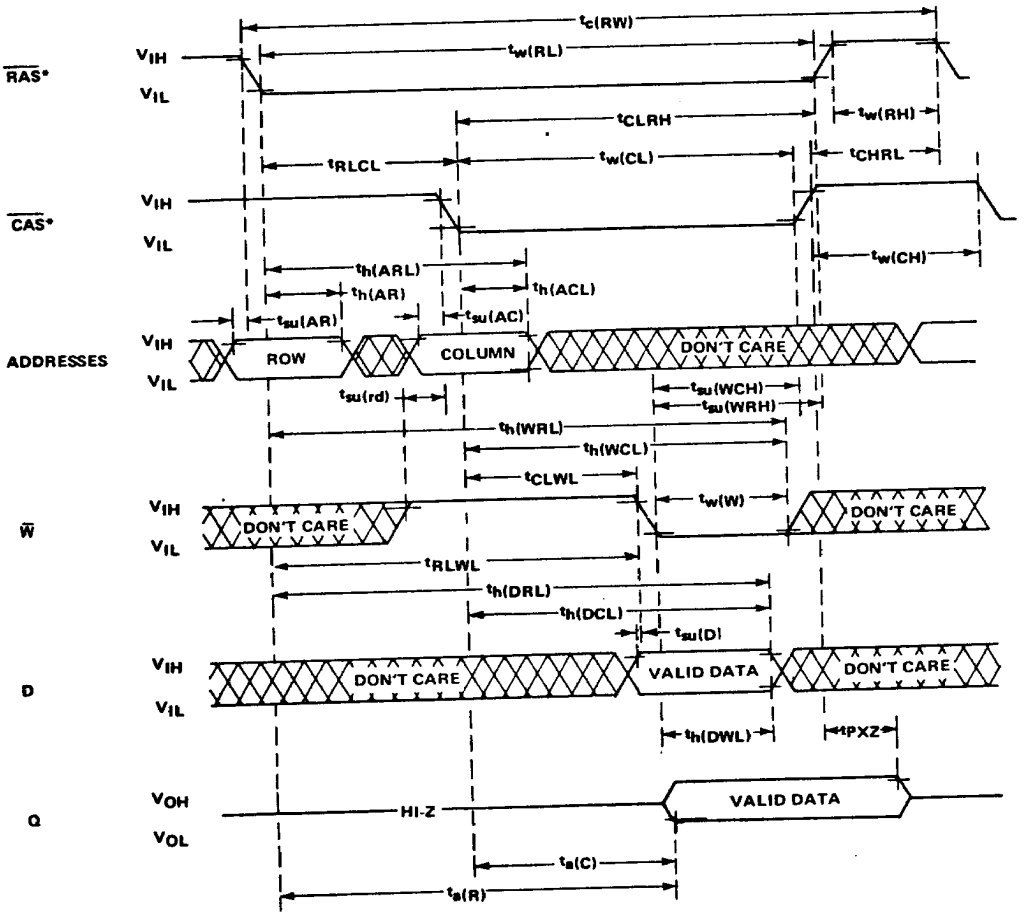
write cycle timing



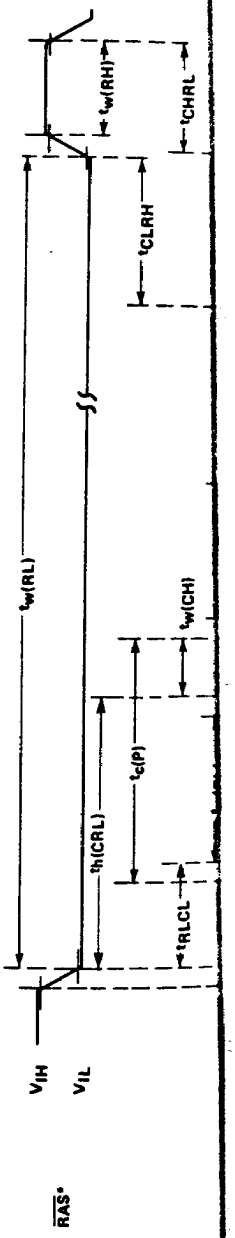
*If module 1 is selected these are $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ remain high.
If module 2 is selected these are $\overline{RAS}2$ and $\overline{CAS}2$, $\overline{RAS}1$ and $\overline{CAS}1$ remain high.

read-write/read-modify-write cycle timing

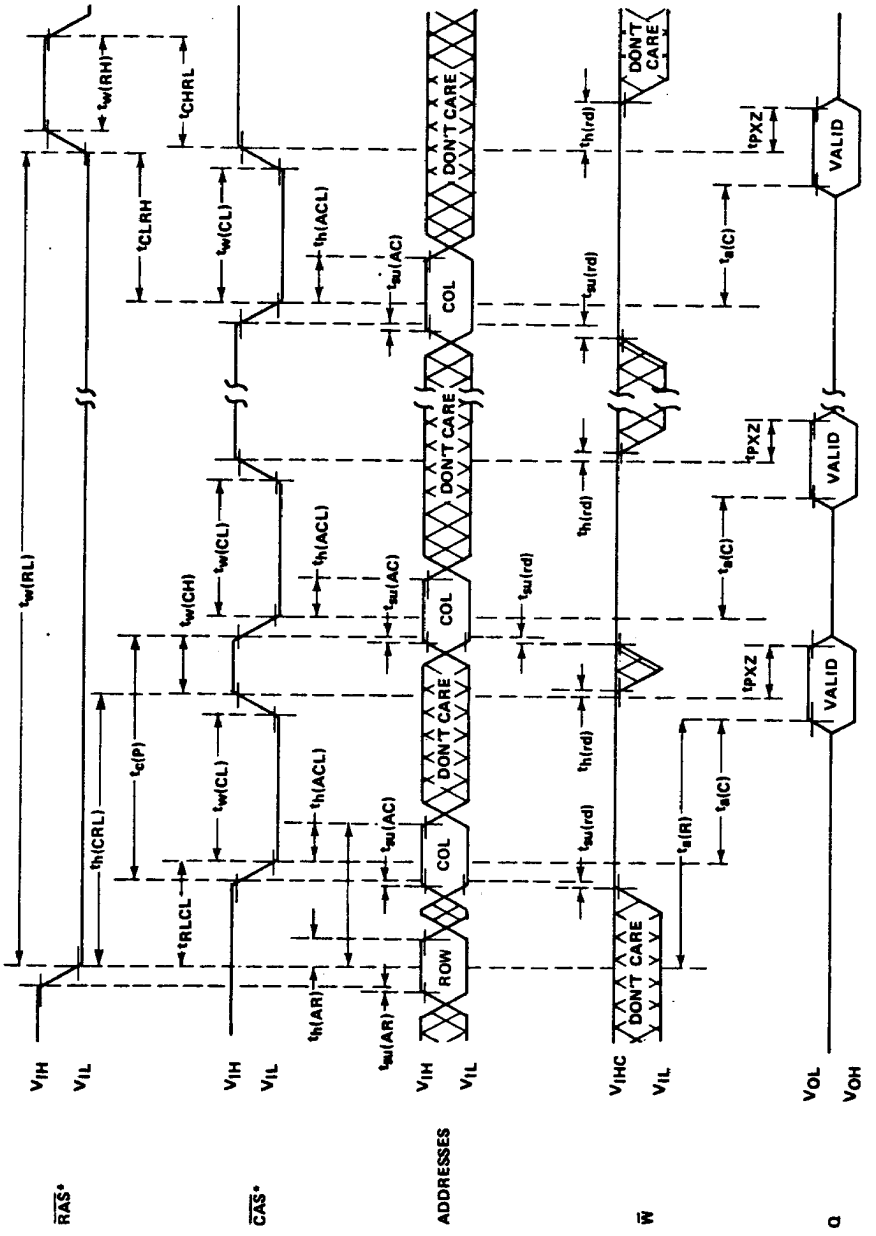


*If module 1 is selected these are $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ remain high.
If module 2 is selected these are $\overline{RAS}2$ and $\overline{CAS}2$, $\overline{RAS}1$ and $\overline{CAS}1$ remain high.

page-mode read cycle ti

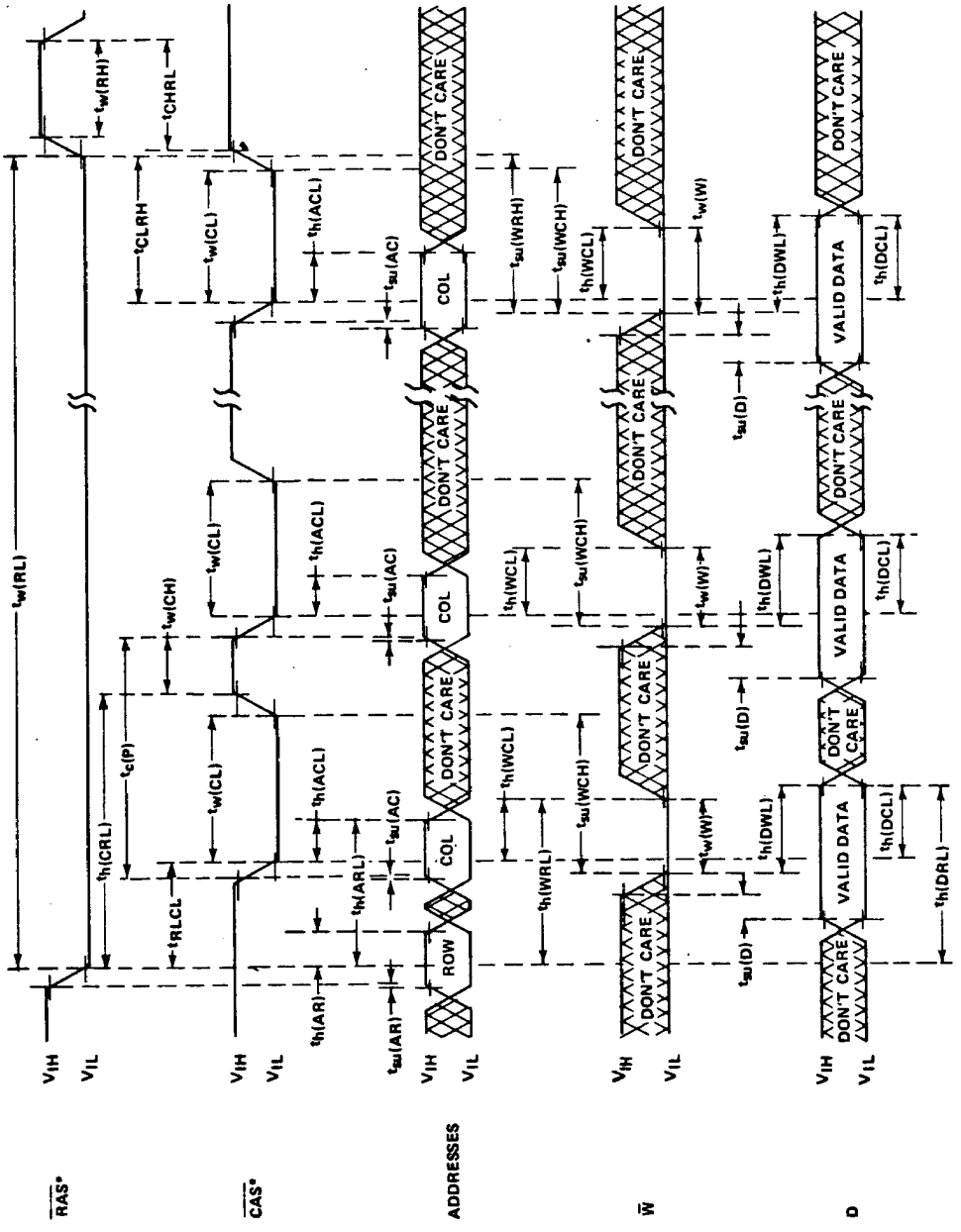


page-mode read cycle timing



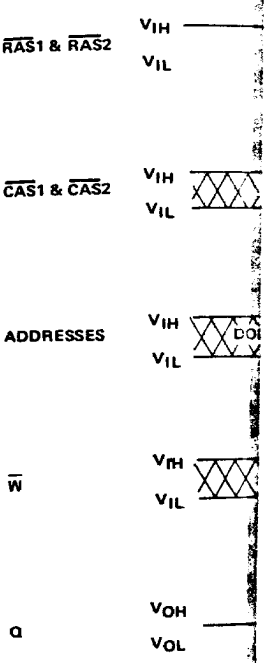
*If module 1 is selected these are $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ remain high.
If module 2 is selected these are $\overline{RAS}2$ and $\overline{CAS}2$, $\overline{RAS}1$ and $\overline{CAS}1$ remain high.

page-mode write cycle timing



*If module 1 is selected these are $\overline{RAS}1$ and $\overline{CAS}1$, $\overline{RAS}2$ and $\overline{CAS}2$ remain high.
If module 2 is selected these are $\overline{RAS}2$ and $\overline{CAS}2$, $\overline{RAS}1$ and $\overline{CAS}1$ remain high.

$\overline{RAS}$-only refresh timing



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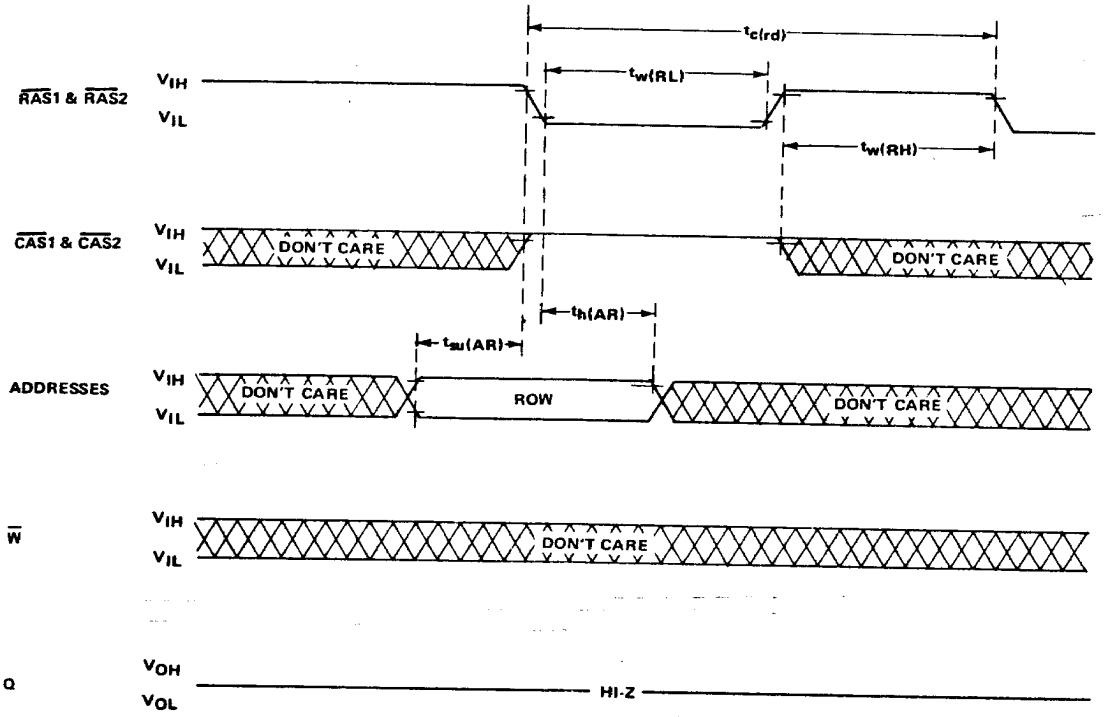
$\overline{RAS}$-only refresh timing



*If module 1 is selected these are $\overline{RAS1}$ and $\overline{CAS1}$, $\overline{RAS2}$ and $\overline{CAS2}$ remain high.
If module 2 is selected these are $\overline{RAS2}$ and $\overline{CAS2}$, $\overline{RAS1}$ and $\overline{CAS1}$ remain high.