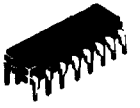
HM51256 Series

262144-word × 1-bit CMOS Dynamic Random Access Memory

HM51256P Series



(DP-16B)

HM51256CP Series

(CP-18)

HM51256ZP Series

(ZP-16)

■FEATURE

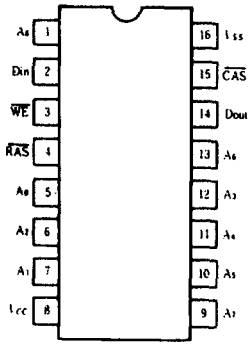
- 262, 144 word x 1 bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 85/100/120/150ns
  - Address access time: 40/45/55/70ns
- Cycle time
  - Random read/write cycle time: 155/180/210/250ns
  - High speed page mode cycle time: 50/55/65/80ns
- Lower power
  - Standby: 11mW (TTL Level)
    1.1mW (CMOS Level: L-version)
  - Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
  256 cycles/32ms (L-version)
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control

■ ORDERING INFORMATION

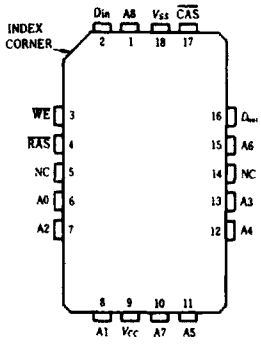
Type No.	Access Time	Package
HM51256P-8	85ns	300 mil 16 pin Plastic DIP
HM51256P-10	100ns	
HM51256P-12	120ns	
HM51256P-15	150ns	
HM51256CP-8	85ns	18 Pin PLCC
HM51256CP-10	100ns	
HM51256CP-12	120ns	
HM51256CP-15	150ns	
HM51256LP-8	85ns	300 mil 16 pin Plastic DIP
HM51256LP-10	100ns	
HM51256LP-12	120ns	
HM51256LP-15	150ns	
HM51256LCP-8	85ns	18 pin PLCC
HM51256LCP-10	100ns	
HM51256LCP-12	120ns	
HM51256LCP-15	150ns	
HM51256ZP-8	85ns	16 pin Plastic ZIP
HM51256ZP-10	100ns	
HM51256ZP-12	120ns	
HM51256ZP-15	150ns	
HM51256LZP-8	85ns	
HM51256LZP-10	100ns	
HM51256LZP-12	120ns	
HM51256LZP-15	150ns	

■ PIN ARRANGEMENT

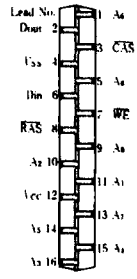
- HM51256P Series
- HM51256CP Series
- HM51256ZP Series



(Top View)



(Top View)



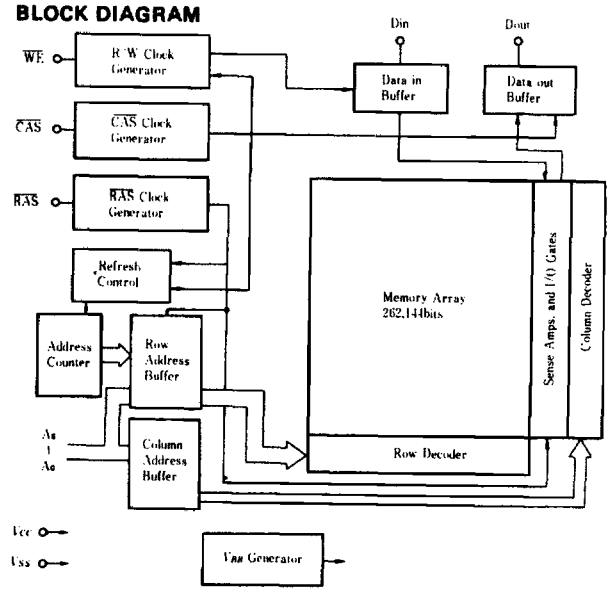
(Bottom View)

A_8-A_0	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_6-A_7	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$= V_{IH}, Dout=High Impedance)	I_{CC2}	–	2	–	2	–	2	–	2	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	–	70	–	60	–	50	–	40	mA	
Standby Current ($\overline{RAS}$= V_{IH}, Dout Enable)	I_{CC4}	–	6	–	6	–	6	–	6	mA	1
Refresh Current ($\overline{CAS}$ before RAS Refresh, t_{RC}=min)	I_{CC5}	–	60	–	55	–	45	–	35	mA	
High Speed Page Mode Supply Current ($\overline{RAS}$= V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=min.)	I_{CC6}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$, $\overline{CAS}$= Vcc−0.2V)	I_{CC7}	–	200	–	200	–	200	–	200	μA	2
Input leakage (0< V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage (0< V_{out}<7V, Dout=Distable)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}= −5mA)	V_{OH}	2.4	Vcc	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. This specification is guaranteed only for L-version.

■CAPACITANCE (Vcc=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1
Output Capacitance	Data-out	C_O	–	7		1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$= V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	–	25	–	30	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	–	75	–	90	–	110	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
		–	32	–	32	–	32	–	32	ms	21

● Read Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10

● Refresh Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Prechange to $\overline{CAS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	50	–	55	–	65	–	80	–	ns	18, 20
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	55	75000	65	75000	75	75000	95	75000	ns	19
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSH}	90	–	105	–	125	–	155	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	20	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	
Access Time from Column Precharge Time	t_{CAP}	–	45	–	50	–	60	–	75	ns	20

● High Speed Page Mode Read-Modify-Write Cycle

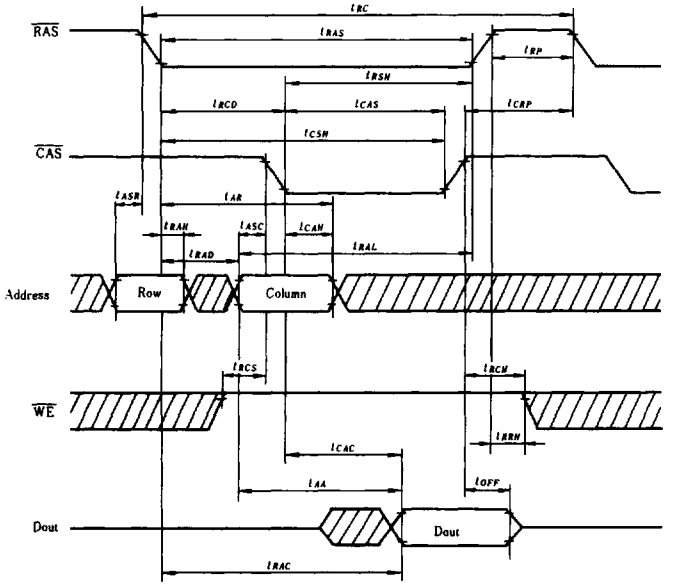
Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value show in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a Reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWPC} (min) = t_{AWD} (min) + t_{WAD} (max) + t_T.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If t_{WAD} is greater than the maximum recomended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the t_{WAD} (max) limit insures that t_{PWA} (max) can be met, t_{WAD} (max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. An intial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
17. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. Assumes that $t_{ASC} = t_{CP} - 5$ ns.
19. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
20. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
21. This specification is guaranteed only for L-version.

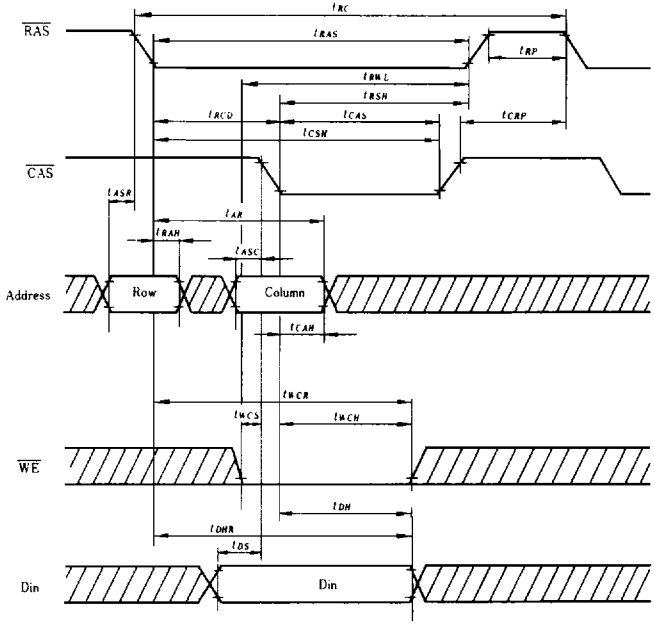
■TIMING WAVEFORMS

●Read Cycle



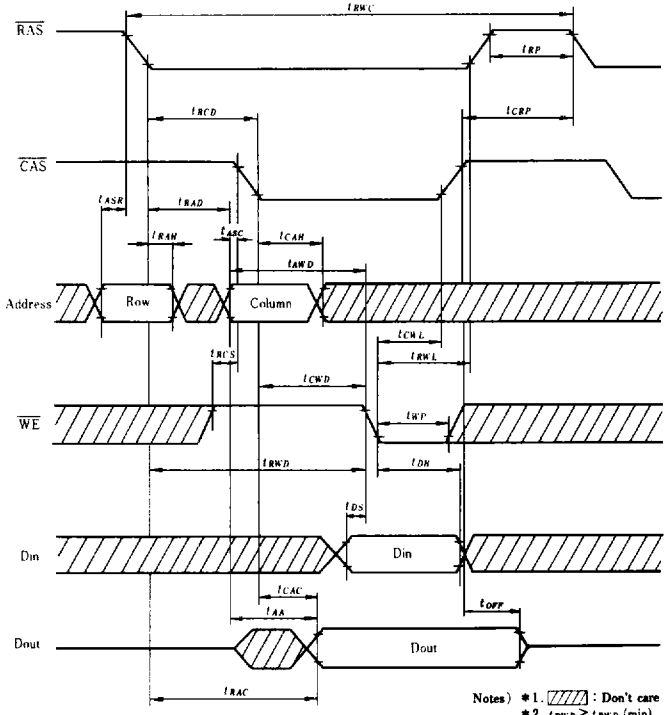
Note) ▨ : Don't care

● Write Cycle



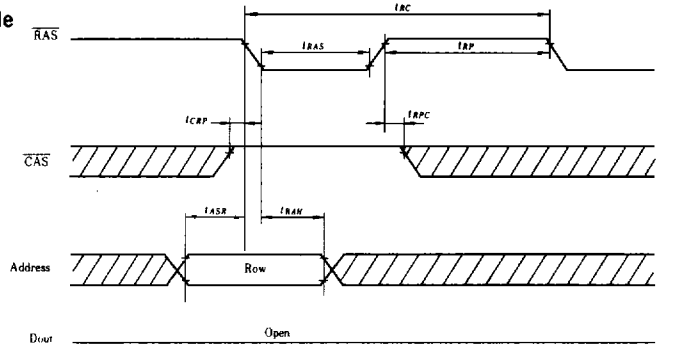
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● Read Modify Write Cycle



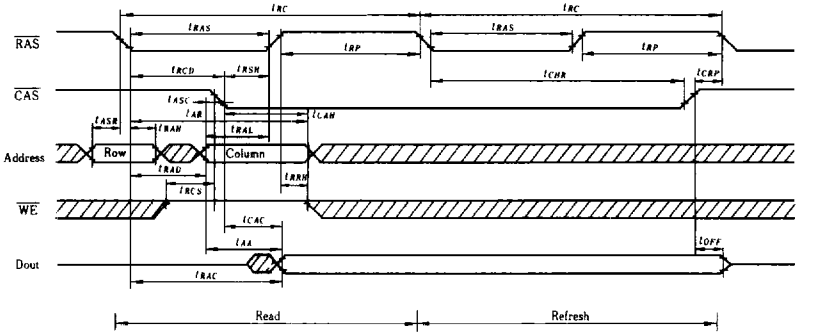
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$ (min)
$t_{CWD} \geq t_{CWD}$ (min)
$t_{AWD} \geq t_{AWD}$ (min)

● $\overline{RAS}$ Only Refresh Cycle



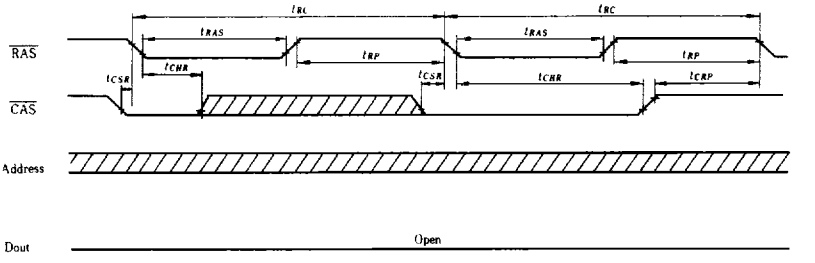
Note) ▨ : Don't care

● Hidden Refresh Cycle



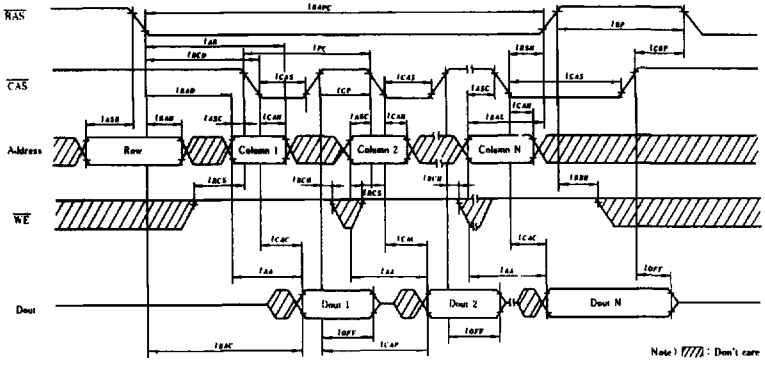
Note) ▨ : Don't care

● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



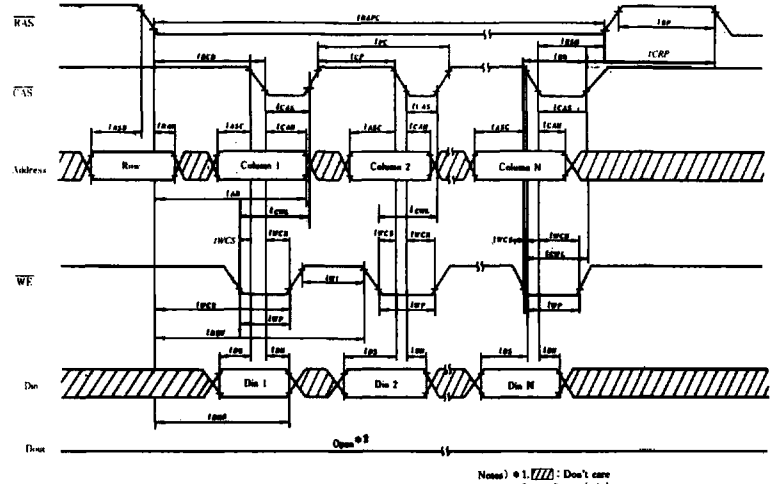
Note) ▨ : Don't care

● High Speed Page Mode Read Cycle



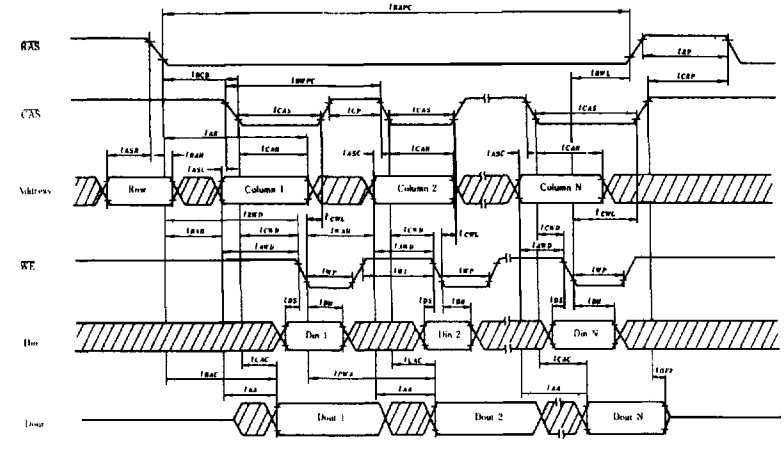
Note) ▨ : Don't care

● High Speed Page Mode Write Cycle



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● High Speed Page Mode Read Modify Write Cycle



Note) ▨ : Don't care