OKI semiconductor

MSM3716-AS/RS

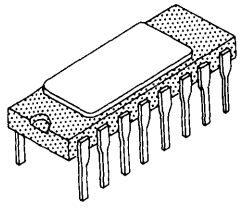
16384 WORD X 1 BIT DYNAMIC RAM

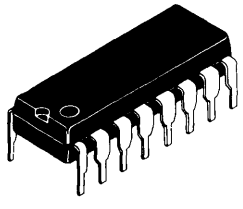
GENERAL DESCRIPTION

The Oki N-MOS integrated circuit MSM3716- x AS/RS is an address multiplex type dynamic RAM with a 16,384 word x 1-bit configuration, featuring a wide operational margin and high-speed low power consumption while using a single transistor.

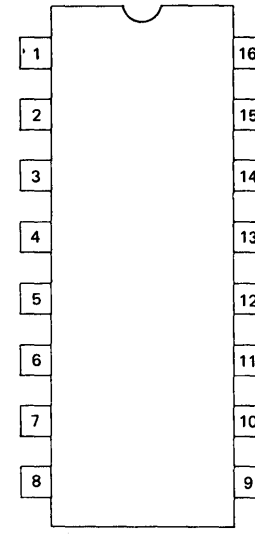
FEATURES

- 16,384 words x 1 bit
- 150ns access time and 375ns cycle time (MSM3716-2AS/RS)
  200ns access time and 375ns cycle time (MSM3716-3AS/RS)
- Standard 16-pin layout
- Low power consumption: 528mW (operation), 20mW (standby)
- Output data controlled by $\overline{CAS}$ only, while system design freedom is increased by not latch at cycle end.
- Read modify write, $\overline{RAS}$ only refresh and page mode operations possible.
- TTL compatible low capacitance for all inputs.
- 128 refresh cycle.





PIN CONFIGURATION



1	V_{BB}	9	V_{CC}
2	D_{IN}	10	A_5
3	$\overline{WRITE}$	11	A_4
4	$\overline{RAS}$	12	A_3
5	A_0	13	A_6
6	A_2	14	D_{OUT}
7	A_1	25	$\overline{CAS}$
8	V_{DD}	16	V_{SS}

9

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Respect to Vss	−1.0 ~ +15.0	V
	Vcc		−1.0 ~ +15.0	
	V_{BB}	Respect to Vss V_{DD} − Vss > 0 · 0	0 ~ −20.0	
	V_{DD}	Respect to V_{BB}	−0.5 ~ +20.0	
	Vcc		−0.5 ~ +20.0	
	Vss		−0.5 ~ +20.0	
Input voltage	V_I	Respect to V_{BB}	−0.5 ~ +20.0	
Output voltage	V_O		−0.5 ~ +20.0	
Storage temperature	Tstg		−55 ~ +150	°C
Permissible loss	P_D		1	W

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Conditions	Recommended Operating Conditions			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{DD}	Vss = 0	10.8	12.0	13.2	V
	V_{CC}		4.5	5.0	5.5	
	V_{BB}		−4.5	−5.0	−5.5	
"H" clock input voltage (note 1)	V_{IHC}		2.7		6.0	
"H" input voltage (note 2)	V_{IH}		2.4		6.0	
"L" input voltage (note 3)	V_{IL}		−1.0		0.8	
Operating temperature	Topr		0		70	°C

Notes: 1. $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$ inputs
2. A_0 ~ A_6 and D_{IN} inputs
3. All inputs

9

DC CHARACTERISTICS

(V_{DD} = 12.0V±10%, Vcc = 5.0V±10%, V_{BB} = −5.0V±10%, Vss = 0V, Ta = 0~70°C)

Item	Symbol	Conditions	Special Ratings		Unit	Note
			Min.	Max.		
Average power supply current during operation	I_{DD1}	t_{RC} = 375 ns		40	mA	4
	I_{CC1}					5
	I_{BB1}			200	μA	
Power supply current during standby mode	I_{DD2}	$\overline{RAS}$ = V_{IHC}		1.5	mA	
	I_{CC2}	D_{OUT} = High Impedance	−10	10	μA	
	I_{BB2}			100	μA	
Refresh power supply current	I_{DD3}	t_{RC} = 375 ns		27	mA	4
	I_{CC3}		−10	10	μA	
	I_{BB3}			200	μA	
Page mode power supply current	I_{DD4}	$\overline{RAS}$ = V_{IL}		29	mA	4
	I_{CC4}	t_{PC} = 225 ns				5
	I_{BB4}			200	μA	
Input leak current	I_{L1}	V_{BB} = −5V $0 \leq V_I < 6.0V$	−10	10	μA	
Output leak current	I_{LO}	D_{OUT} = Disable $0 \leq V_O \leq 5.5V$	−10	10	μA	
"H" output voltage	V_{OH}	I_O = −5 mA	2.4		V	
"L" output voltage	V_{OL}	I_O = 4.2 mA		0.4	V	

Notes: 4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle time.
5. I_{CC1} and I_{CC4} are changed by output load. Vcc is connected to D_{OUT} at low impedance during reading of "H" level data.

9

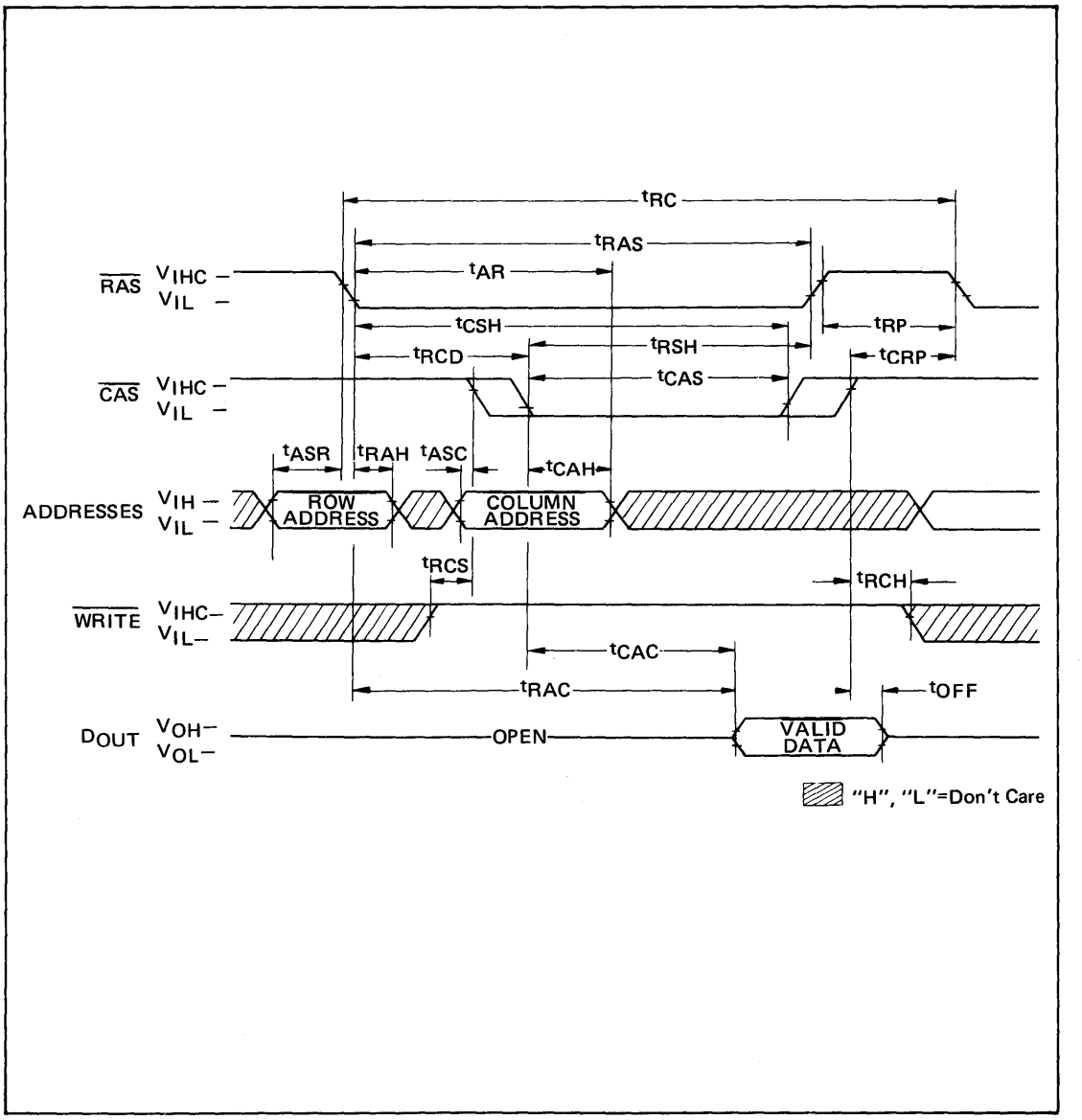
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 12.0V±10%, Vcc = 5.0V±10%, V_{BB} = −5V±10%, Vss = 0V, Ta = 0~70°C) (Notes; 6, 7. 8)

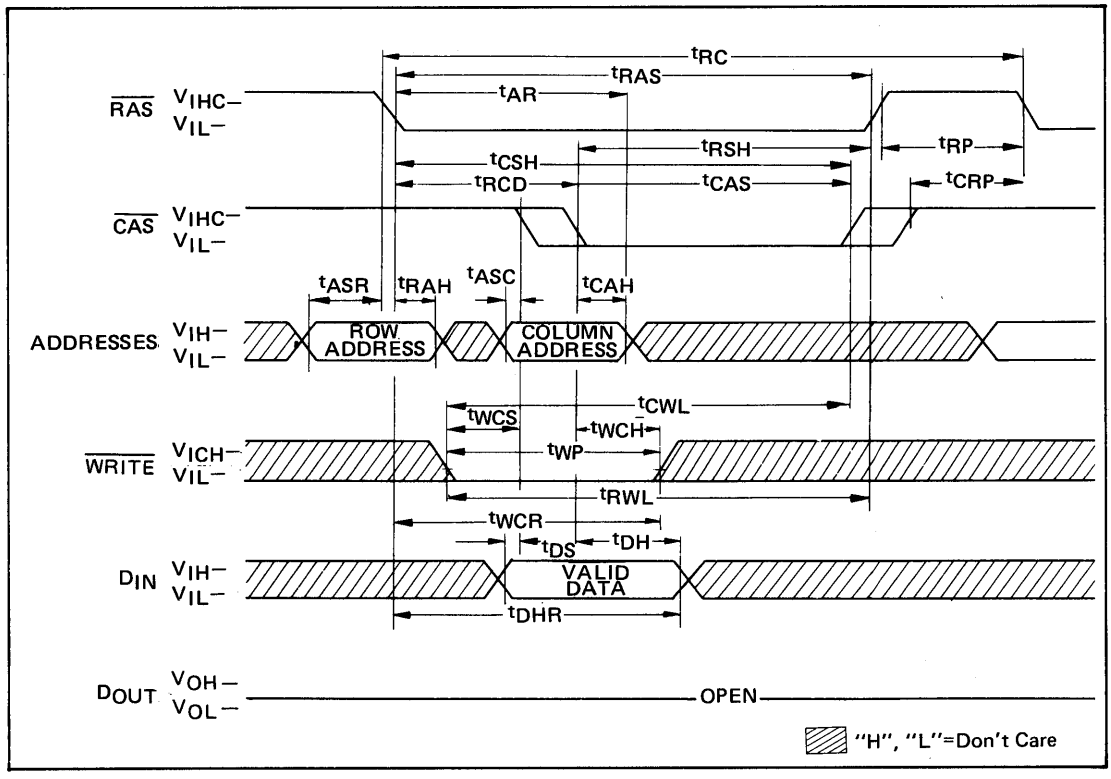
Parameter	Symbol	MSM3716-2AS/RS		MSM3716-3AS/RS		Units	Note
		Min.	Max.	Min.	Max.		
Random read/write cycle time	t_{RC}	375		375		ns	
Read and write cycle time	t_{RWC}	375		375		ns	
Page mode cycle time	t_{PC}	170		225			
Access time from $\overline{RAS}$	t_{RAC}		150		200		9, 11
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	10, 11
Output turn-off delay time	t_{OFF}	0	40	0	50	ns	
Rise and fall time	t_T	3	35	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$ and $\overline{CAS}$ delay time	t_{RCD}	25	50	30	65	ns	12
$\overline{RAS}$ and $\overline{CAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	20		25		ns	
Column address set-up time	t_{ASC}	−5		−5		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time from $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command and $\overline{RAS}$ read time	t_{RWL}	60		80		ns	
Write command and $\overline{CAS}$ read time	t_{CWL}	60		80		ns	
Data input set-up time	t_{DS}	0		0		ns	13
Data input hold time	t_{DH}	45		55		ns	13
Input hold time for data from $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time	t_{CP}	60		80		ns	
Write command set-up time	t_{WCS}	−20		−20		ns	14
$\overline{CAS}$ and write command delay time	t_{CWD}	70		95		ns	14
$\overline{RAS}$ and write command delay time	t_{RWD}	120		160		ns	14
Refresh cycle	t_{REF}		2		2	ms	

NOTES: 6. Normal memory operation may not be possible unless at least 8 cycles of operation are performed after the power is switched on.
7. AC measurements when t_T = 5ns.
8. Prescribed timing input levels of V_{IHC} (MIN), V_{IH} (MIN) and V_{IL} (MAX).
9. In the case of $t_{RCD} \leq t_{RCD}$ (MAX); t_{RAC} is increased only for $t_{RCD} - t_{RCD}$ (MAX) for $t_{RCD} > t_{RCD}$ (MAX) case.
10. For $t_{RCD} \geq t_{RCD}$ (MAX) case.
11. For 2TTL + 100pF load case.
12. t_{RCD} (MAX) is the value guaranteed by t_{RAC} (MAX), and when $t_{RCD} > t_{RCD}$ (MAX) it is distributed by t_{CAC}.
13. t_{DS} and t_{DH} are specified by the $\overline{CAS}$ falling edge during the write cycle (early write), and by the $\overline{WRITE}$ falling edge during read modify write cycle.
14. t_{WCS}, t_{CWD} and t_{RWD} are not parameters specifying operational limits.
$t_{WCS} \geq t_{WCS}$ (MIN) results in write cycle (early write) with high impedance output.
$t_{CWD} \geq t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN) result in read modify write cycle.

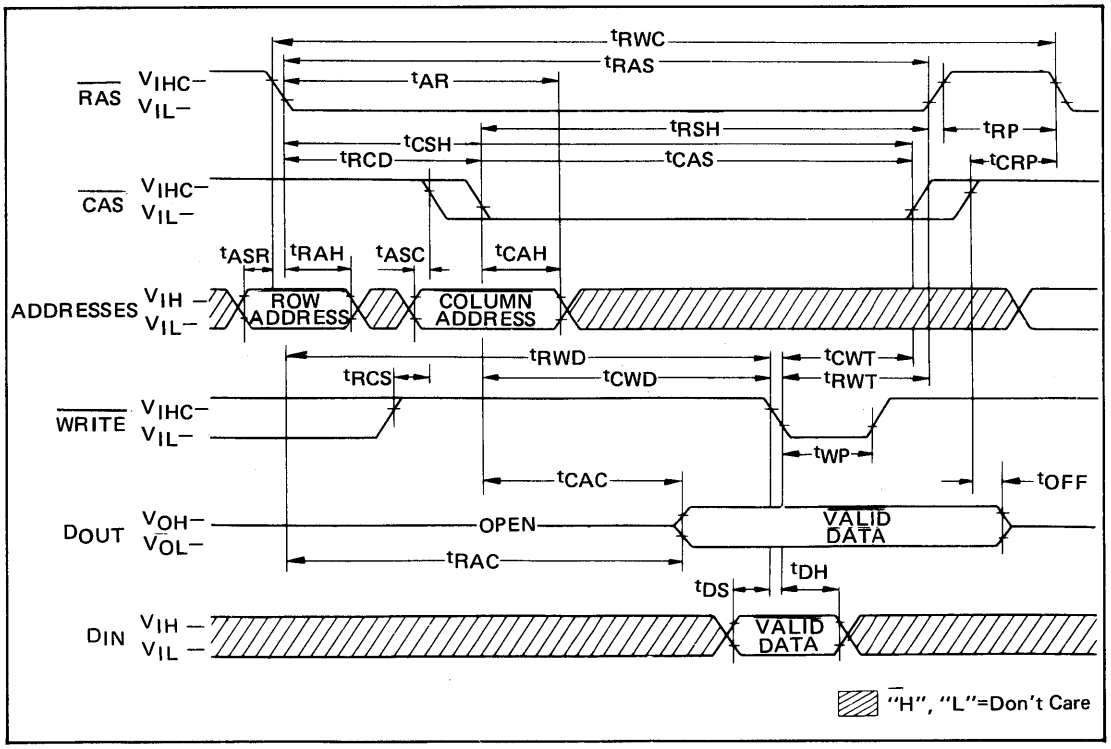
READ CYCLE



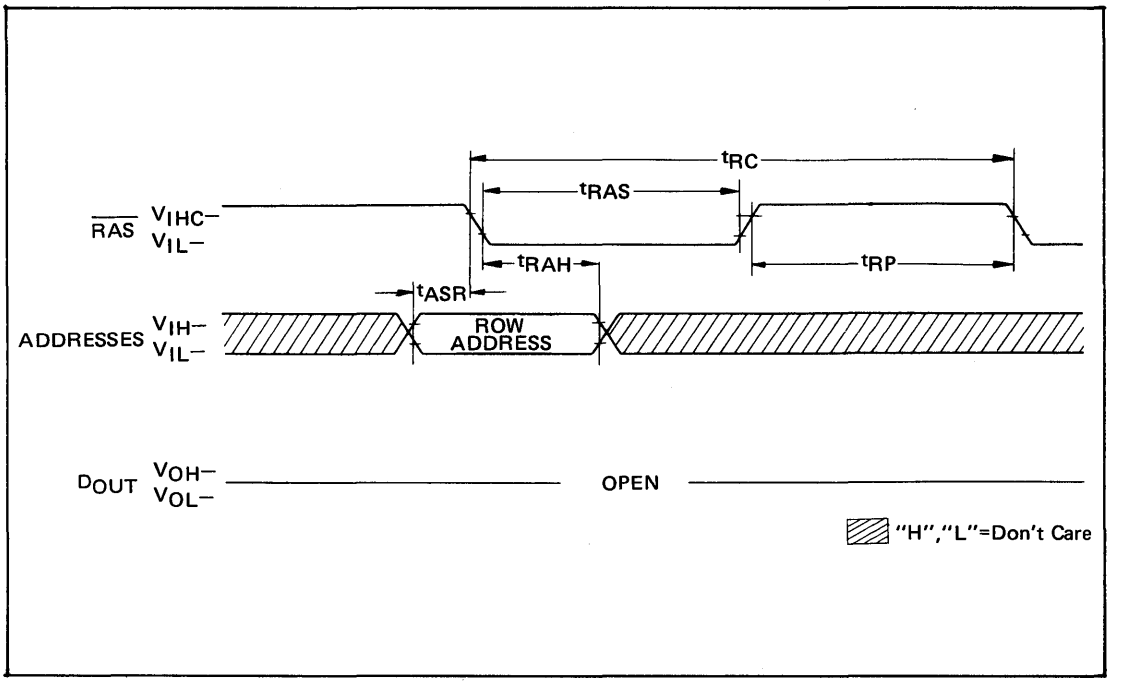
WRITE CYCLE (EARLY WRITE)



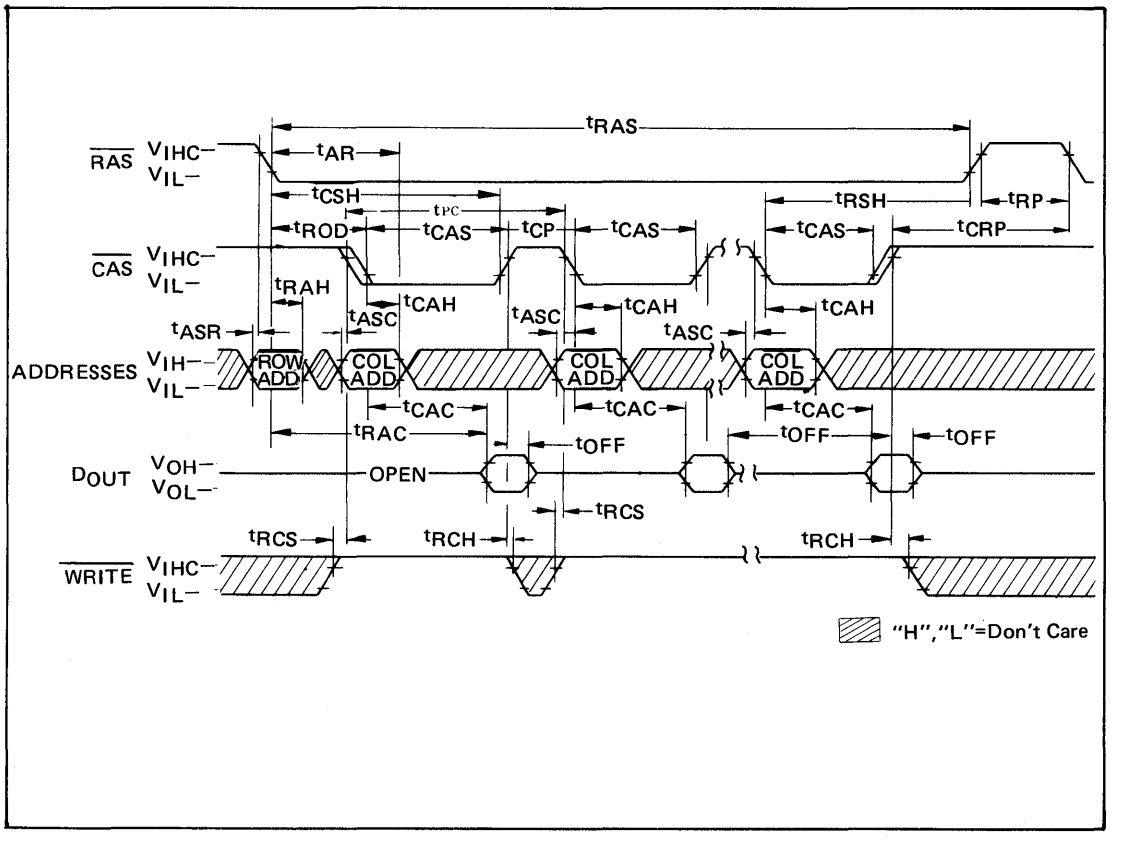
READ-WRITE/READ-MODIFY-WRITE CYCLE



"$\overline{RAS}$-ONLY" REFRESH CYCLE $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE



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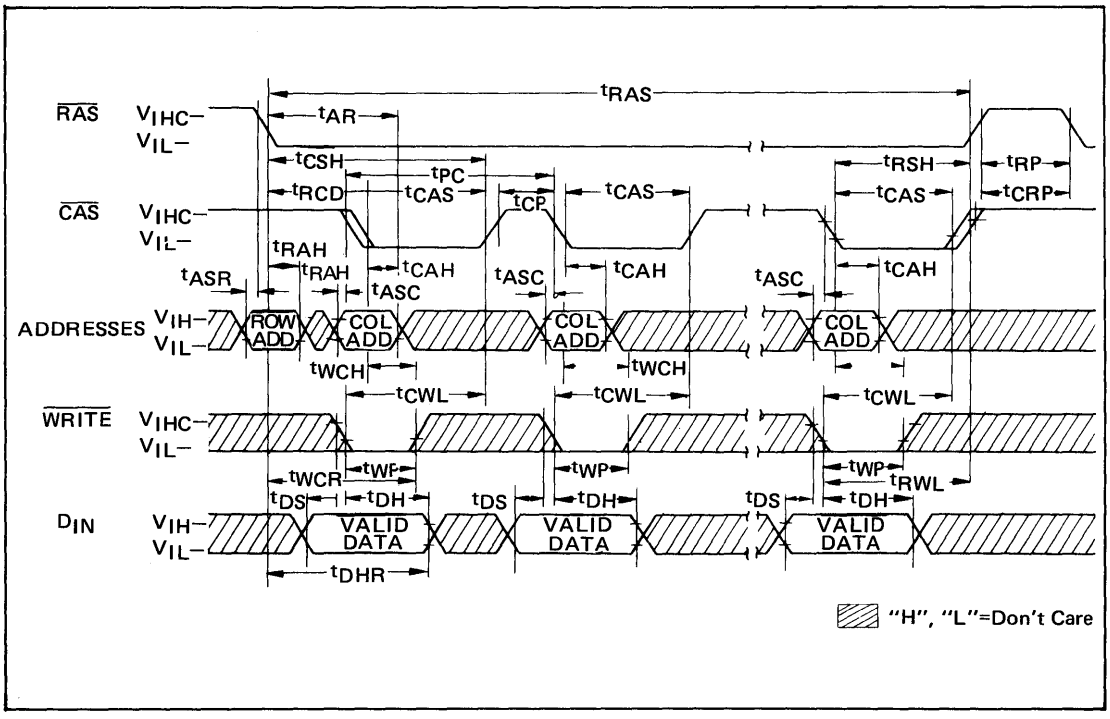
PAGE MODE WRITE CYCLE



TERMINAL CAPACITY CHARACTERISTICS

(V_{DD} = 12.0V ± 10%, V_{SS} = 0V, V_{BB} = 5.0V ± 10%, Ta = 0 ~ 70°C)

		Standard	Maximum	Unit	Remarks
Input capacity (A_0~A_6, D_{IN})	C_1	4	5		
Input ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	C_1	8	10	pF	
Output capacity (D_{OUT})	C_0	5	7		$\overline{CAS}$=V_{IHC}

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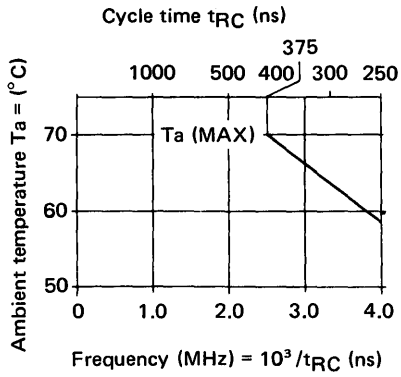
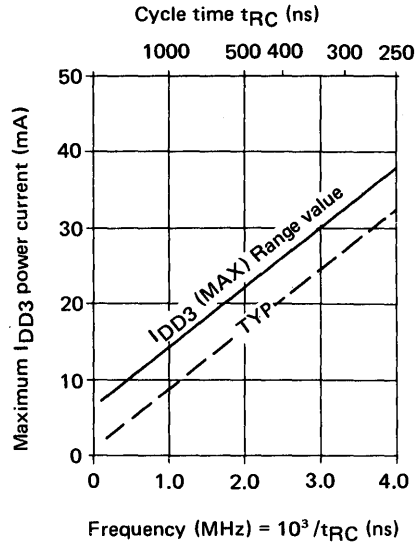
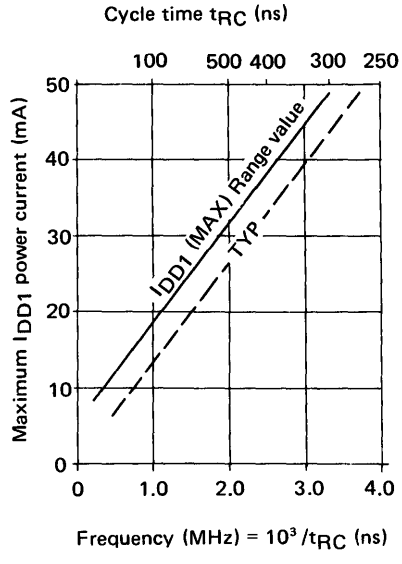
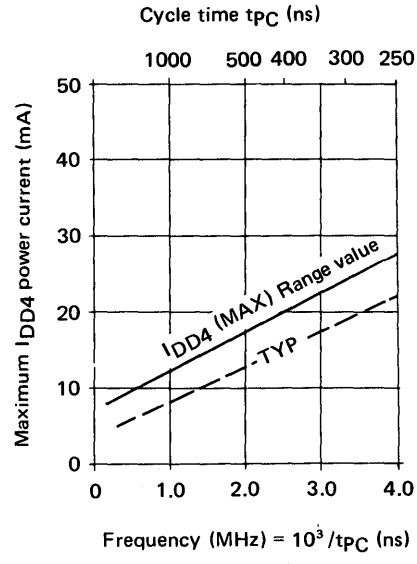
TYPICAL CHARACTERISTICS









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