LASER™

TURBO XT

Technical Reference Manual

(The following is applicable to U.S.A. FCC class B version only)

This equipment generates and uses radio frequency energy. If it is not installed and used properly, that is, in strict accordance with the manufacturer's instructions, it may cause interference to radio and television reception.

It has been tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J, Part 15, of FCC Rules. These rules are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the computer with respect to the receiver
- Move the computer away from the receiver
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits

If necessary, you should consult the dealer or an experienced radio/television technician for additional suggestions. You may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve Radio-TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, DC20402, Stock No. 004-000-00345-4.

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CHAPTER 1

OVERVIEW

1. Overview

1.1 Assembly of the computer

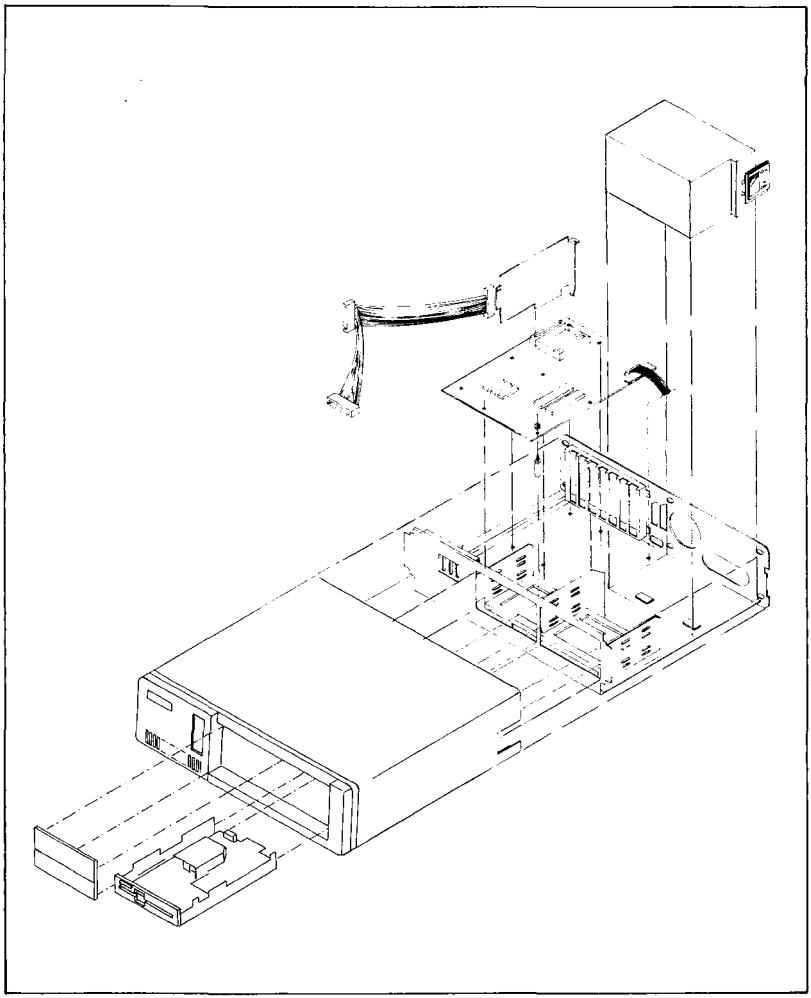


Fig. 1.1 Exploded view of the computer

1.2 System Board Diagram

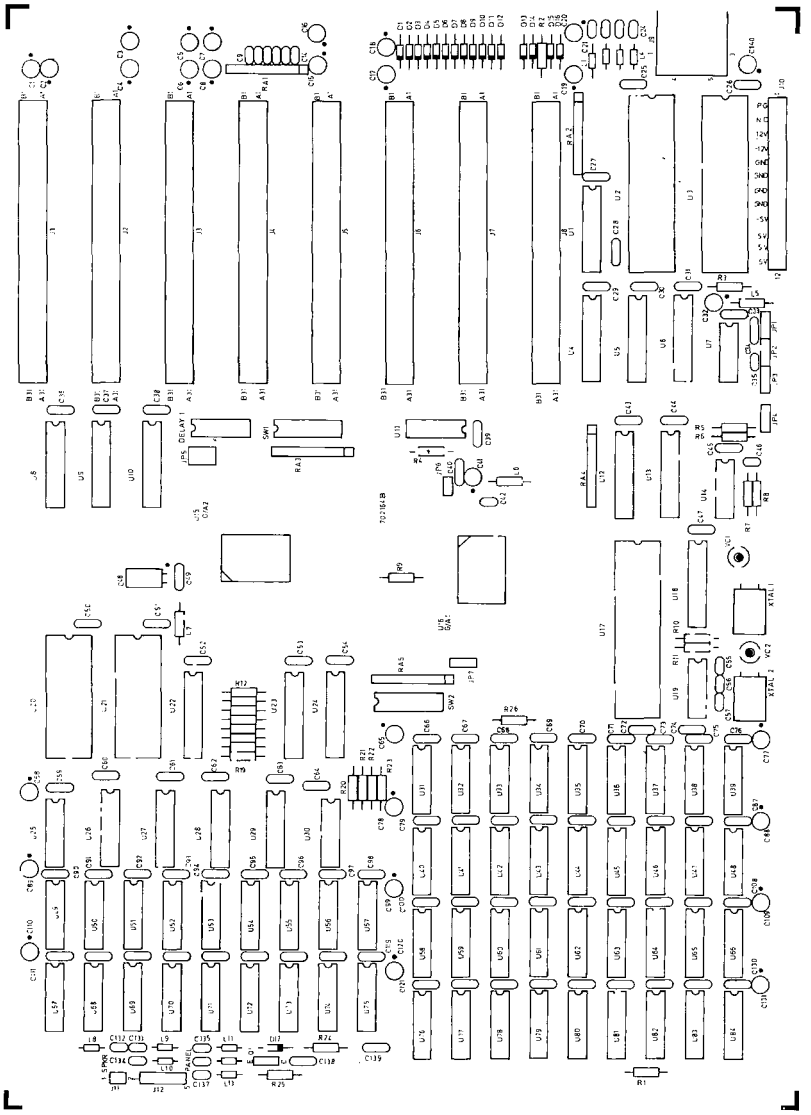


Fig. 1.2 System board diagram

1.3 Power Supply

The system DC power supply is a switching regulator, it is designed to operate at 130 watts continuously. The supply provides 4 voltage levels, they are 15A of +5V DC. 4.2A of +12V DC, 300 mA of -5V DC and 300 mA of -12V DC. If DC over-load or over-voltage conditions exist, the supply will automatically be shuted down. The AC input is also fused.

1.4 Keyboard

The keyboard layout resembles an ordinary typewriter. There are two types of keyboards offered to the users. One has 84 keys and the other is the XT enhanced keyboard with 101/102 keys. Most of the keys share the same functions. These two types of keyboards are detachable and interface to the main units via a 5 pin DIN type connector through a spiral cable.

1.5 Disk Drive

The computer system can accommodate two double-sided and double-density disk drives.

The disk drive capacity is as follow:

Unformatted	Formatted
Media 500K Bytes	Media 360K Bytes
Track 6520 Bytes	Track 4608 Bytes

These two disk drives communicate with the main board via a Disk Drive Controller card or a Multi-I/O Card.

The number of disk drives installed should be set by setting the DIP switch DIP-SW1 properly according to the following diagram.

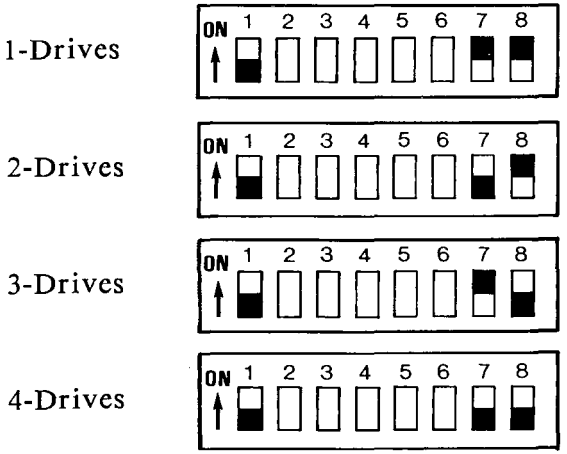


Fig. 1.3 DIP switch settings for disk drives

1.6 Front Panel

On the front panel there is a keyboard lock. When the lock is on, all characters typed on the keyboard will be ignored.

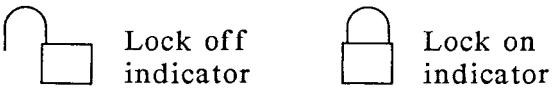


Fig 1.4 Keyboard Lock Indicator

There are also a power indicator and a high speed indicator. When the LED of the high speed indicator is lit, the CPU is running at high speed mode.

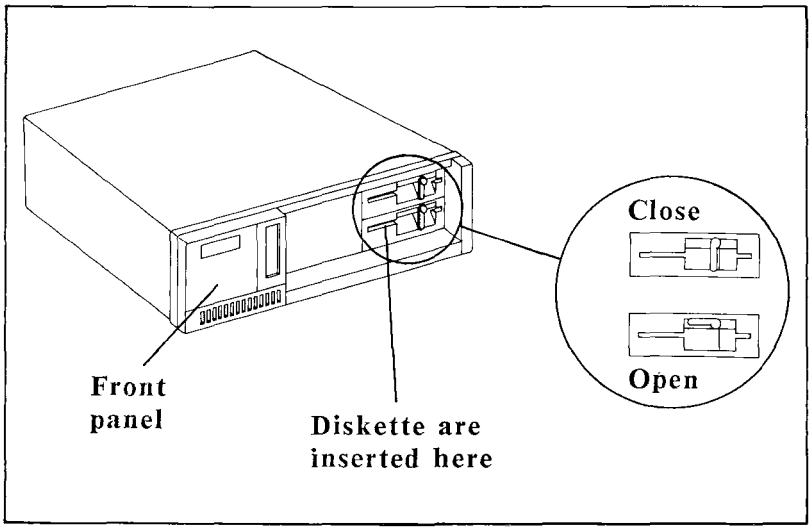


Fig 1.5 Front Panel

CHAPTER 2

SYSTEM BOARD

2. SYSTEM BOARD

2.1 Block Diagram

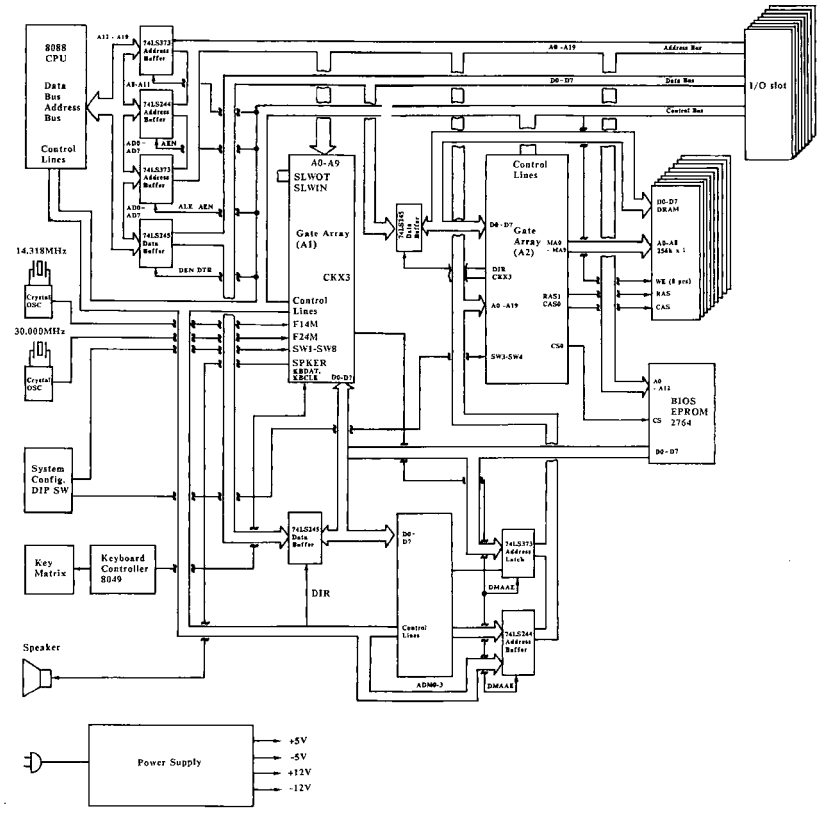


Fig. 2.1 System board block diagram

2.2 Microprocessor

The CPU of Laser Turbo XT is the Intel® 8088-1 (or 8088-2 in the 8MHZ model) it is a high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin DIP package.

The Intel® 8088-1 have the following features:

- 8-bit data bus interface
- 16-bit internal architecture
- Direct addressing capability to 1 Mbyte of memory
- Direct software compatibility with 8086
- 14-word by 16-bit register set with symmetrical operations
- 24 operand addressing modes
- Byte, word and block operations
- 8-bit and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
- Clock rate of 10 MHZ.

On the Turbo XT, the 8088-1 can be driven at two Clock speed - 4.77MHz and 10 MHz. At 4.77MHz, memory accesses take four Clock cycles (840ns). While I/O accesses take five clock cycles (1050ns). At 10 MHz, the internal RAM accesses take four cycles (400ns) while all other memory accesses take 5 cycles. (500ns) I/O accesses still take 5 cycles. However, the clock is slowed down to 4.77MHz for all I/O accesses. The same is true for DMA cycles. This ensure the turbo XT is compatible with most expansion cards when running even at 10 MHz which is more than twice the normal speed.

2.3 Coprocessor

An 8087 numeric data coprocessor can be installed on the TURBO XT to provide instructions and data types needed for high performance numeric applications.

The 8087 is a numeric processor extension that performs arithmetic and logical instruction on many types of numeric data. It also executes many built-in transcendental functions. The 8087 is treated as an extension to the CPU, providing register, data types, control, and instruction capabilities at the hardware level. The programmers can treat the CPU and the 8087 as a single processor.

The 8087 is offered in three versions:

- the 8087 (5MHz)
  8087-2 (8MHz)
  8087-1 (10MHz)

The 8088-1 must be used if the computer is to be operated at 10 MHz.

2.4 RAM (Random - access memory)

The computer have 640K of RAM on board located at the bottom left corner. At the bottom right corner, there are 4 rows of sockets for the expanded memory. The layout of RAM on PCB is shown on Fig 2.2.

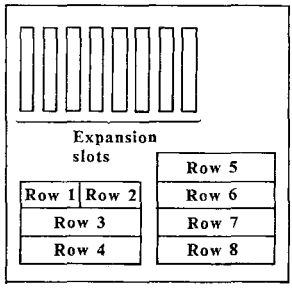
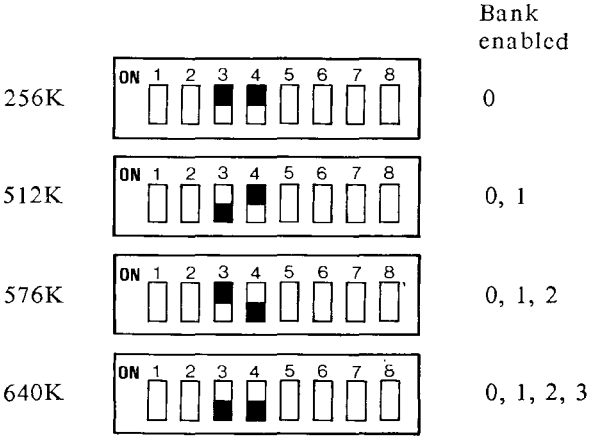


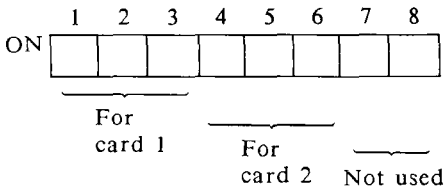
Fig 2.2 Layout of RAM on PCB

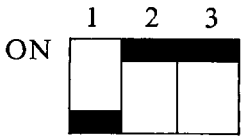
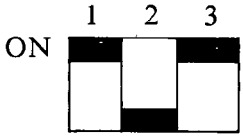
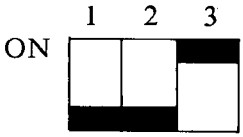
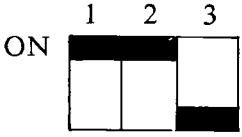
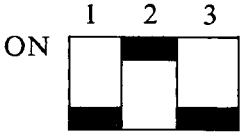
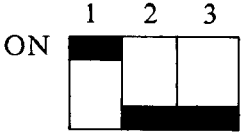
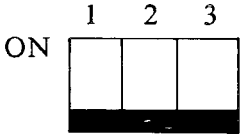
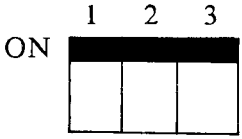
Row 1 and Row 2 both make up of two 4464 and one 4164, Row 3 and Row 4 are two row of 41256, these four rows of RAM make up totally 640K of memory on board. These portion of RAM that the DOS can recognize is known as conventional memory. For the amount of conventional memory installed on board the DIP switch SW1 should be set properly according to the following diagram.



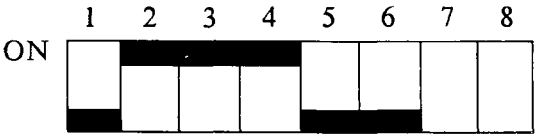
Row 5 to Row 8 are four row of socekts for expanded memory. They should be inserted with 41256 and start inserting from Row 5. When all sockets are inserted with 41256, the total expanded memory will be 1Mbyte.

For the amount of expanded memory installed, the DIP switch SW2 should be set properly. You may imagine that there are two expanded memory cards installed on the mainboard. The first consists of Row 5 and Row 6. The other consists of Row 7 and Row 8. Each card has a set of I/O ports for control purposes. The addresses of these I/O ports must be unique for each card. A 8 pole DIP switch is used to set these addresses.



DIP switch setting	I/O port address (in Hex)
	208
	218
	258
	268
	2A8
	2B8
	2E8
	Disable the on board expanded memory

For example, the following DIP-switch setting configures card 1 at address 208H and card 2 at 2B8H.

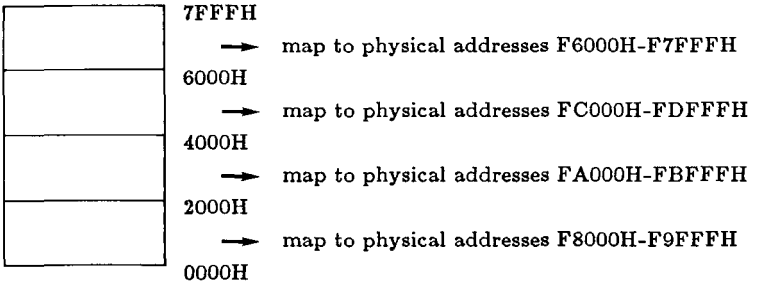


The access time of the DRAM chips has to be 150ns or less for 8MHz high speed speration. For the 10MHz model 120ns DRAM is required.

2.5 ROM (Read only memory)

There are two 28-pin sockets for ROM, one of them is occupied by a 2764 which stored the BIOS (Basic Input Output system). The other empty socket is used to house a 32K ROM, such as the BASIC ROM.

The contents of the BASIC ROM should be arranged as follows.



2.6 Interrupt Subsystem

There are eight prioritized levels of interrupt, six are available on the system expansion slots for use by expansion cards. Two levels are used on the system board. Level 0 is connected to channel 0 of the timer to provide a periodic interrupt for the time-of-day clock.

Level 1 is used by the keyboard interface. Whenever a scan code from the keyboard is received an interrupt will be initiated.

The non-maskable interrupt (NMI) of the 8088 is connected to the memory parity checking circuitry. It is also used by the 8087 coprocessor to report errors. Fig 2.3 is the listing of the system interrupt.

Number	Usage
NMI	Parity 8087
0	Timer
1	Keyboard
2	EGA
3	RS232 COM2
4	RS232 COM1
5	Hard disk
6	Diskette
7	Printer

Fig 2.3 Hardware interrupt listing

The interrupt controller and NMI circuitry are integrated into the gate array A1.

2.7 DMA (Direct Memory Access)

The Turbo XT employ a 8237A-5 Direct Memory Access (DMA) controller to perform the DMA function.

The 8237A-5 contains 344 bits of internal memory in the form of registers. Fig 2-4 is the listing of these registers.

Name	Size (bit)	No.
Base Address Registers	16	4
Base Word Count Registers	16	4
Current Address Registers	16	4
Current Word Count Registers	16	4
Temporary Address Register	16	1
Temporary Word Count Register	16	1
Status Register	8	1
Command Register	8	1
Temporary Register	8	1
Mode Registers	6	4
Mask Register	4	1
Request Register	4	1

Fig 2.4 8237A-5 internal registers

The 8237 only provides 16 bits of address A0-A15. An additional DMA page register is used to provide the highest 4 bits of addresses A16-A19 so that the entire 1M address space can be accessed. The DMA page register is located at gate array A2.

The following figure shows the addresses of the DMA page register.

I/O address	R/W	Register
81H	W	Page register for DMA channel 2
82H	W	Page register for DMA channel 3
83H	W	Page register for DMA channel 1

Fig 2.5 DMA page register.

The DMA channel 0 is normally reserved for the function of dynamic RAM refreshing.

2.8 Timer

The Programmable Interval Timer is integrated in the gate array A1 and have the register set shown below.

I/O address	R/W	Register
40H	R/W	Counter 0
41H	R/W	Counter 1
42H	R/W	Counter 2
43H	W	Counter Word

Fig 2.6 Programmable interval timer register set.

Counter 0 is used as a general purpose timer. Counter 1 is used to count and request refresh cycles. Counter 2 is used as a tone generation for the loudspeaker. All timer are clocked at 1.19MHz.

2.9 CPU Speed Control Port

The CPU speed control port is a R/W register with address 1F0H. The first seven bits of the register is not used. Bit 7 is used to set the speed mode of the computer, when its content is 0, the CPU is running at standard speed (4.77MHz). When its content is 1, the CPU is running at high speed mode.

2.10 Expanded Memory

The gate array A2 can supports three Expanded Memory Boards (Only two are used on the Turbo XT) with each one contains a maximum of 2 Mbyte RAM. 1 Mbit DRAM can be supported while 41256 can also be used. On the TURBO XT four Row of 41256 are used to provide a total of 1Mbytes of Expanded Memory.

Each Expanded Memory Board is controlled via eight I/O ports. The addresses of these ports are determined by external DIP switches settings. ESWO-ESW2 **determine address of board 0 while ESW3-ESW5 for board 1 and ESW6-ESW8 for board 2. (ESW6 & ESW8 are shorted to ground on the Turbo XT).

Fig 2.7 Summarizes the DIP switches settings and the corresponding Page Mapping Register and Control Register for the Expanded Memory Board.

ESW2 ESW5 ESW8	ESW1 ESW4 ESW7	ESW0 ESW3 ESW6	Page Mapping Register	Control Register
0	0	0	Expaned memory disabled	
0	0	1	0208H, 4208H, 8208H, C208H	0209H, 4209H, 8209H, C209H
0	1	0	0218H, 4218H, 8218H, C218H	0219H, 4219H, 8219H, C219H
0	1	1	0258H, 4258H, 8258H, C258H	0259H, 4259H, 8259H, C259H
1	0	0	0268H, 4268H, 8268H, C268H	0269H, 4269H, 8269H, C269H
1	0	1	02A8H, 42A8H, 82A8H, C2A8H	02A9H, 42A9H, 82A9H, C2A9
1	1	0	02B8H, 42B8H, 82B8H, C2B8H	02B9H, 42B9H, 82B9H, C2B9H
1	1	1	02E8H, 42E8H, 82E8H, C2E8H	02E9H, 42E9H, 82E9H, C2E9H

Fig 2.7 The relation between DIP switches settings and the corresponding Page Mapping Register and Control Register for the Expanded Memory Board.

The expanded memory occupy 64K of contiguous memory space. The starting address is determined by the Control Register. Fig 2.8 shows the relation between bit 7 of the control Registers and the starting address.

Bit 7 of 82 x 9H	Bit 7 of 42 x 9H	Bit 7 of 02 x 9H	Starting address
0	0	0	C4000H
0	0	1	C8000H
0	1	0	CC000H
0	1	1	D0000H
1	0	0	D4000H
1	0	1	D8000H
1	1	0	DC000H
1	1	1	E0000H

X=0, 1, 5, 6, A, B, E

Bit 7 of C2X9 must be set to 0. If bit 7 is set to 1, a subsequent read of Expanded Memory will initiate a parity error. This is for testing purpose only.

The Expanded Memory is accessed in 16K page. There are four Page Mapping Registers used to enabling, disabling, and swapping the various pages in and out of the system memory space. Each board can support up to 128 pages, thus using 7 of these 8 bits in each Page Mapping Register. The eighth bit is a page enable/disable bit when set (1 or high), it allows the page to appear in the memory space. When clear (0 or low), the page does not appear in the memory space. This enabling/disabling is necessary to avoid read conflicts between different boards in the system. Fig 2.9 shows the relation between the Page Mapping Register and the corresponding 16K memory window.

I/O address	R/W	16K window
02X8H	R/W	Y0000-Y3FFFH
42X8H	R/W	Y4000-Y7FFFH
82X8H	R/W	Y8000-YBFFFH
C2X8H	R/W	YC000-YFFFFH

X=0,1,5,6,A,B,E
Y is a don't care

Fig 2.9 Relation between Page Mapping Register and the corresponding 16K memory Window

For example, if the Expanded Memory starts from address C4000H, then the port 02X8H controls the D000H-D3FFFH window, 42X8H controls the C4000H-C7FFFH window, 82X8H controls the C8000-CBFFFH window and C2X8H controls the CC000H-CFFFFH window.

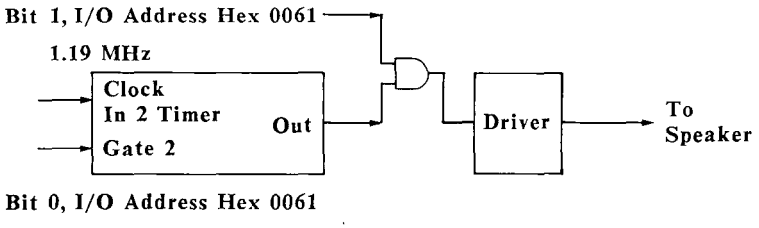
On the LASER TURBO XT, the expanded memory pages are partially decoded. For example, page number 80H and 90H will reference the same page. The details are as follow

RAM Location	Descriptions	
Row 5	Board 0	Page C0H-CFH Partially decoded through C0H-FFH
Row 6	Board 0	Page 80H-8FH Partially decoded through 80H-BFH
Row 7	Board 1	Page C0H-CFH Partially decoded through C0H-FFH
Row 8	Board 1	Page 80-8FH Partially decoded through 80-BFH

2.11 Speaker

The sound system has a small speaker. The speaker can be driven from one or both of two sources:

- An by setting & resetting BIT 1 of I/O port 61H.
- By timer channel, this timer is clocked by a 1.19 MHz clock. The timer gate is also controlled by bit 0 of I/O port 61H.



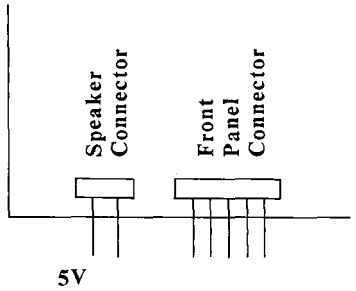


Fig 2.10 Speaker connector.

2.12 Front panel connector

A five pin jumper J12 is situated at the right bottom of the PCB, the pin 1 and pin 2 of the front panel connector are for keyboard lock, if these two pins is open, any data entered from the keyboard will not be recognized.

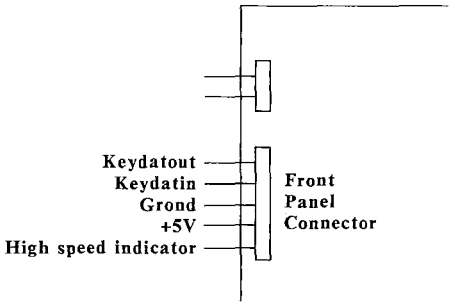


Fig 2.11 Front panel connector

2.13 Memory Map

Start Address Decimal	Start Address Hex	Function
0	00000	256-640K Read/Write Memory on System Board
16K	04000	
32K	08000	
48K	0C000	
64K	10000	
80K	14000	
96K	18000	
112K	1C000	
128K	20000	
144K	24000	
160K	28000	
176K	2C000	
192K	30000	
208K	34000	
224K	38000	
240K	3C000	
256K	40000	
272K	44000	
288K	48000	
304K	4C000	
320K	50000	
336K	54000	
352K	58000	
368K	5C000	
384K	60000	
400K	64000	
416K	68000	
432K	6C000	

Start Address Decimal	Hex	Function
448K	70000	
464K	74000	
480K	78000	
496K	7C000	
512K	80000	
528K	84000	
544K	88000	
560K	8C000	
576K	90000	
592K	94000	
608K	98000	
624K	9C000	
640K	A0000	
656K	A4000	
672K	A8000	128K Reserved
688K	AC000	
704K	B0000	Monochrome
720K	B4000	
736K	B8000	Color/Graphics
752K	BC000	
768K	C0000	EGA BIOS
784K	C4000	
800K	C8000	Fixed Disk Control

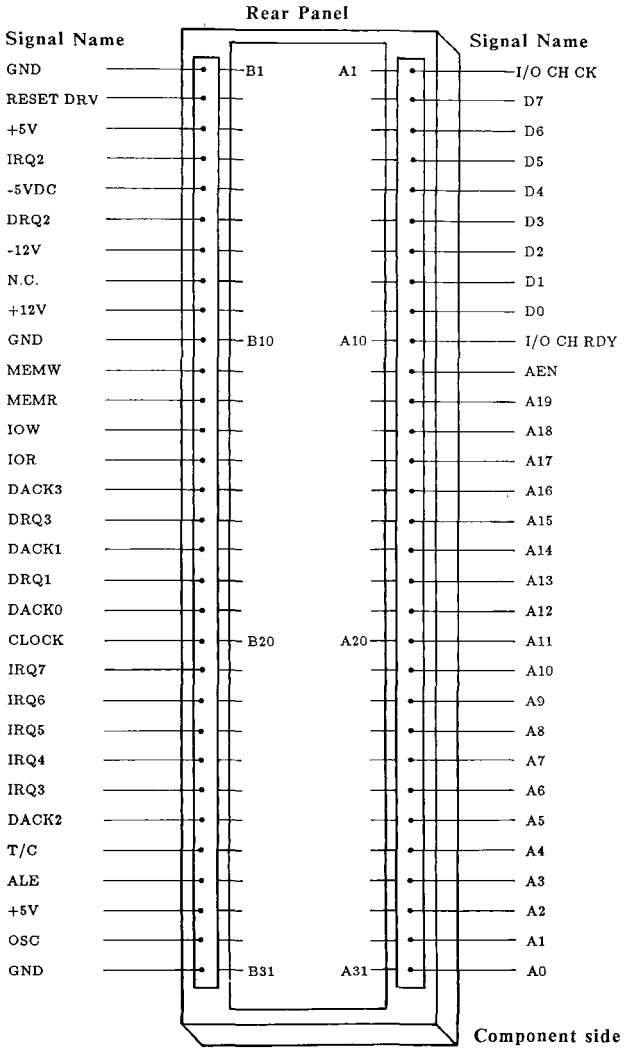
Start Address Decimal	Hex	Function
816K	CC000	
832K	D0000	
848K	D4000	192K Read only
864K	D8000	Memory
880K	DC000	Expansion and
896K	E0000	Control
912K	E4000	
928K	E8000	
944K	EC000	
960K	F0000	
976K	F4000	64K Base System
992K	F8000	ROM
1008K	FC000	BIOS AND BASIC

2.14 I/O MAP

Hex Range	Usage
000-00F	DMA Chip 8237A-5
020-021	Interrupt controller
040-043	Timer
060-063	PPI
080-083	DMA Page Registers
0A0	NMI Mask Register
200-20F	Game Control
210-217	Expansion Unit
2F8-2FF	Asynchronous Communications (Secondary)
300-31F	Prototype Card
320-32F	Fixed Disk
378-37F	Parallel Printer
380-38F	SDLC Communications
3B0-3BF	Monochrome Display Printer
3D0-3DF	Color/Graphics
3F0-3F7	Diskette
3F8-3FF	Asynchronous Communications (Primary)

2.15 I/O Slots

2.15.1 I/O channel diagram



2.15.2 I/O channel signal description

The following is a description of the I/O channel signal. All lines are TTL-compatible.

Signal	I/O	Description
OSC	O	Oscillator : 14.31818 MHz clock. It has a 50% duty cycle.
CLOCK	O	System Clock : It is the CPU clock, it has a period of 210 ns (4.77MHz) in normal mode and a period of 100ns (10MHz) in high speed mode. The clock has a 33% duty cycle.
RESET DRV	O	This line is used to reset system logic on power up or when the line voltage is too low. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address Bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. These lines are generated by either the processor or DMA controller.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices.

Signal	I/O	Description
ALE	O	Address Latch Enable: This line is driven by the bus controller and is used to latch valid addresses from the processor. Processor addresses are latched with the falling edge of ALE.
I/O CH CK	I	I/O Channel Check: When this signal is active low, a parity error is indicated and the NMI signal to the processor will be activated.
I/O CH RDY	I	I/O Channel Ready: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to insert wait states. It allows slower devices to attach to the I/O channel. This line should be asserted immediately when a valid address and the read write command are detected. This line cannot be held longer than 10 clock cycles.

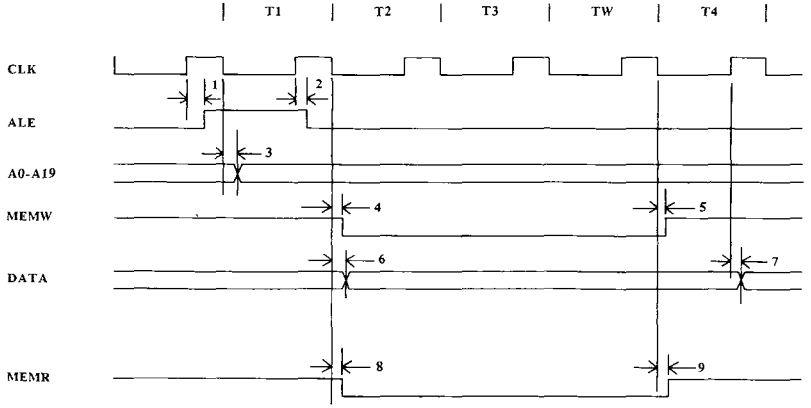
Signal	I/O	Description
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to request services from the processor. IRQ 2 has the highest priority and IRQ7 has the lowest. An interrupt request is generated by asserting an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
IOR	O	-I/O Read Command: This command is used to read data from an I/O device. It may be driven by the processor or the DMA controller. This signal is active low.
IOW	O	-I/O Write Command: This command is used to strobe data into an I/O device. It may be driven by the processor or the DMA controller. This signal is active low.
MEMR	O	Memory Read Command: This command line is used to read a memory. It may be driven by the processor or the DMA controller. This signal is active low.
MEMW	O	Memory Write Command: This command line is used to strobe data into a memory. It may be driven by the processor or the DMA controller, this signal is active low.

Signal	I/O	Description
DRQ1-DRQ3	I	DMA Request 1 to 3: These lines are used to request DMA service, DRQ 3 has the lowest priority and DRQ1 has the highest. A request is generated by asserting a DRQ line to high. A DRQ line must be held high until the corresponding DACK line goes active.
DACK0-DACK3	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3). They are active low. Dack0 is used to refresh dynamic RAM.
AEN	O	Address Enable: When this signal is high, the address bus, data bus and read-write command lines are driven by the DMA controller.
T/C	O	Terminal Count: When the terminal count for any DMA channel is reached, a pulse will be output on this line. This signal is active high.

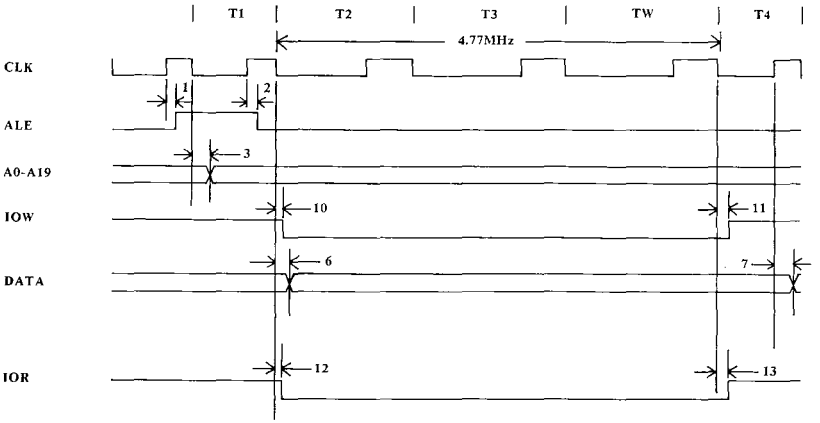
2.15.3 I/O SLOT TIMING at high speed

(Vcc = 5V +/-5%, Ta = 0 To 70°C)

		Min (ns)	Type (ns)	Max (ns)
1.	ALE active delay from CLK	17		84
2.	ALE inactive delay from CLK	2		15
3.	A0-A19 delay from CLK			72
4.	MEMW active delay	4	12	25
5.	MEMW inactive delay	2	8	17
6.	D0-D7 (write) delay			71
7.	D0-D7 (write) delay			58
8.	MEMR active delay	4	12	25
9.	MEMR inactive delay	2	8	17
10.	IOW active delay	4	12	25
11.	IOW inactive delay	2	8	17
12.	IOR active delay	4	12	25
13.	IOR inactive delay	2	8	17



MEMR AND MEMW TIMING AT HIGH SPEED MODE



IOR AND IOW TIMING AT HIGH SPEED MODE

CHAPTER 3

KEYBOARD

3. KEYBOARD

3.1 Keyboard Layout

There are two types of keyboards offered to the users. One has 84 keys while the other is the XT enhanced keyboard with 101/102 keys.

To describe the keyboard clearly, it has been divided into three section according to their different functions.

1 : Typewriter key and control keys
2 : Numeric Keypad and edit keys
3 : Function keys.

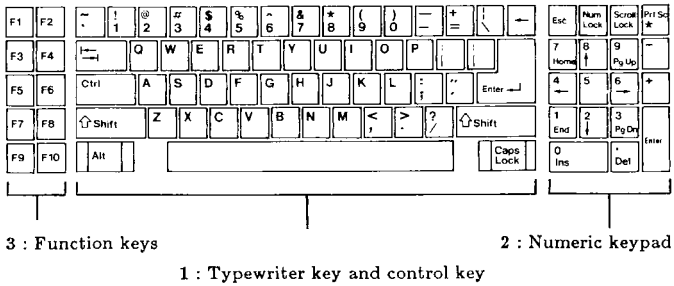


Fig 3.1 Layout of 84 keys keyboard.

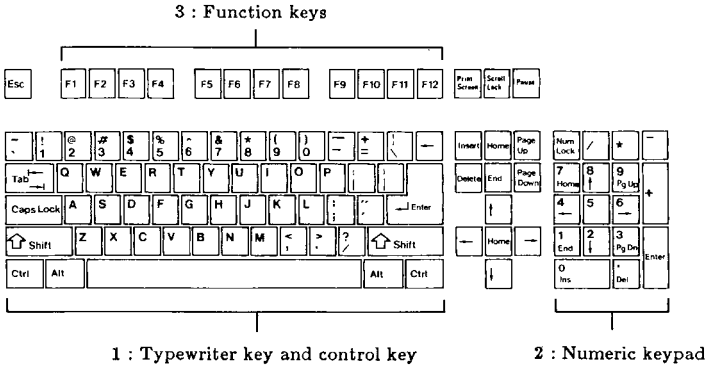


Fig 3.2 Layout of 102 keys keyboard.

3.2 Keyboard Connector

3.2.1 keyboard Connector Specification

The keyboard connector is a 5-pin DIN connector, its pin assignment is illustrated in Fig. 3.3

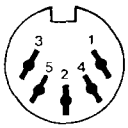


Fig 3.3 Pin assignment of the 5-pin DIN connector

The keyboard connector specification is as follow:

Pin	TTL Signal
1	+Keyboard Clock
2	+Keyboard data
3	-Keyboard Reset
	(Not Used)
4	Ground
5	+5 Volts

3.2.2 Keyboard Connector Signal Description

There are totally five signal lines connecting the keyboard controller to the LASER Turbo XT mainboard.

They are :

(1)	KBDATA	-	Keyboard data
(2)	KBDCLK	-	Keyboard clock
(3)	KRES	-	Keyboard reset
(4)	GND	-	Signal ground
(5)	Vcc	-	+5V DC Supply.

KRES line is not used (N.C.) in the current circuit KBDATA line is a bi-directional line driven by open-collector devices. It is normally low when no signal is transferring.

KBDCLK line is a bi-directional line driven by open-collector devices. It is normally high when no signal is transferring.

3.3 SCAN CODES

3.3.1 Scan Codes Description

On the Laser Turbo XT, as the other IBM PC/XT compatible machines, the keyboard controller is responsible for generating "Scan code" instead of ASCII code. These Scan codes are arbitrary assigned and their meaning are interpreted by the system BIOS or the application programs running. This allows for easy modification to support foreign language keyboards.

Scan codes are classified as "Make" and "Break" codes. Make/Break codes of the same key only differs in the most significant bit (Bit 7). Make code has MSB=0, while Break code has MSB=1.

Not all possible scan code are recognized by the system BIOS. Some invalid scan codes are ignored by the system BIOS, and some forbidden scan code produces "beep" sound when the system BIOS detects it.

"Make" codes are generated when a key is depressed, i.e, changes from OFF state to ON state. If the key is depressed for a certain length of time (Say 1/2 second), the same "Make" code as above will be generated and transmitted to the main unit at a rate of approximately 10 times each second. This "autorepeating" feature is also known as "typmatic".

All the keys on the conventional IBM® PC/XT keyboard are typmatic, however, some keys on the Enhanced Keyboard are not typmatic, i.e, make codes are generated when the key is pressed for the first time, but holding the key down will not generate any further make codes (e.g. Pause key in Enhanced Keyboard).

"Break" codes are generated when a key is released, i.e, changes from ON state to the OFF state.

The delay time before typmatic occurs is approximately 1/2 second. Typmatic rate is approximately 10 codes (code sequence in multi-code conditions) per second. That is, after you have pressed the key and hold down for 1/2 seconds, there will be 10 characters per second generated on the screen.

3.3.2 Scan Codes Details

Terminology used:

1.	CAPS LOCK ON	=	The CAPS LOCK LED IS ON. ie, the main unit interpretes capital letter.
2.	CAPS LOCK OFF	=	The CAPS LOCK LED IS OFF. ie, the main unit interpretes small case letter.
3.	Ctrl ON	=	The Ctrl key (either left or right) is already depressed and not yet released.
4.	Ctrl OFF	=	The Ctrl key is not depressed.

5.	SHIFT ON	=	The Shift key (either, left or right) is already depressed and not yet released.
6.	SHIFT OFF	=	The shift keys are not depressed.
7.	RIGHT SHIFT ON	=	The right shift key is depressed and not yet released.
8.	LEFT SHIFT ON	=	The left shift key is depressed and not yet released.
9.	ALT ON	=	The Alt key (left or right) is depressed and not yet released.
10.	ALT ON	=	The ALT keys are not pressed.
11.	SCROLL LOCK ON	=	The SCROLL LOCK LED is lighted. (if no such LED, internal status is stored.
12.	SCROLL LOCK OFF	=	The SCROLL LOCK LED is off. (if no such LED, internal status is stored)
13.	NUM LOCK ON	=	The Num Lock LED is lighted. Main unit interpretes numeric keypad as numbers
14.	NUM LOCK OFF	=	The Num Lock LED is off. Main unit interpretes numeric keypad as cursor.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
F1	3B	repeatly 3B	BB
F2	3C	repeatly 3C	BC
F3	3D	repeatly 3D	BD
F4	3E	repeatly 3E	BE
F5	3F	repeatly 3F	BF
F6	40	repeatly 40	C0
F7	41	repeatly 41	C1
F8	42	repeatly 42	C2
F9	43	repeatly 43	C3
F10	44	repeatly 44	C4
F11	57	repeatly 57	D7
F12	58	repeatly 58	D8
ESC	01	repeatly 01	81

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Caps Lock	3A and toggles Caps Lock LED	repeatly 3A and Caps Lock LED unchange	BA and LED Caps Lock unchange
Num Lock	45 and toggles Num Lock LED	repeatly 45 and Num Lock LED unchanged	C5 and Num Lock LED unchange
Ctrl (left)	1D	repeatly 1D	9D
Ctrl (right)	E0, 1D	repeatly E0, 1D	E0, 9D
Alt (left)	38	repeatly 38	B8
Alt (right)	E0, 38	repeatly E0, 38	E0, B8

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
* (Numeric KeyPad)	If SHIFT OFF, then send 37 If either left/right SHIFT ON, send 37. If Both SHIFT ON then send no code.	If SHIFT OFF, repeatly send 37. If either left/right SHIFT ON, repeatly send 37 If Both SHIFT ON then send no code.	If SHIFT OFF, send B7. If either left/right SHIFT ON, send B7 If Both SHIFT ON then send no code.
/ (Numeric Key Pad)	If SHIFT OFF, then send E0,35. If Left SHIFT ON then send E0,AA, E0,35. If Right SHIFT ON, then send E0, B6, E0, 35. If Both SHIFT ON, then send no code.	If SHIFT OFF, repeatly send E0, 35. If either left/right SHIFT ON, repeatly send E0, 35. If Both SHIFT ON then send no code	If SHIFT OFF, send E0, B5 If left SHIFT ON, then send E0, B5, E0, 2A If Right SHIFT ON,then send E0, B5, E0, 36. If Both SHIFT ON, then send no code

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Print Screen (sys Req)	If ALT ON, then send 54. If ALT OFF, If SHIFT OFF, send E0, 2A, E0, 37. If SHIFT ON, send E0, 37.	If ALT ON, repeatly send 54. If ALT OFF, repeat send E0, 37,	If ALT ON send D4, If ALT OFF, Send E0, B7 E0, AA
Scroll Lock	If Ctrl OFF, then send 46, and toggles SCROLL LOCK LED If Ctrl ON, then send 46, and does not toggle SCROLL LOCK LED.	Repeatly send 46	Send C6. SCROLL LOCK LED not affected
Pause (Break)	If Ctrl ON, then send E0, 46, E0, C6. If Ctrl OFF, then send E1, 1D, 45, E1, 9D, C5.	No further code send.	No Code send

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
→	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 4D	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,4D.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, CD.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 4D If Right SHIFT ON, send E0, B6, E0, 4D If Both SHIFT ON, send E0, B6, E0, AA, E0, 4D.	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0, 4D	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, CD, E0, 2A. If Right SHIFT ON, send E0, CD, E0, 36. If Both SHIFT ON, send E0, CD, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 4D	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0, 4D.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, CD, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 4D.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 4D.	case (iv) NUM LOCK ON, SHIFT ON, send E0, CD.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
SHIFT (left)	2A	repeatly 2A	AA
SHIFT (right)	36	repeatly 36	B6
ENTER (Big)	1C	repeatly 1C	9C
Enter (Numeric KeyPad)	E0, 1C	repeatly E0, 1C	E0, 9C
+ (Numeric KeyPad)	4E	repeatly 4E	CE
- (Numeric KeyPad)	4A	repeatly 4A	CA

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Insert	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 52	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,52.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,D2.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 52 If Right SHIFT ON, send E0, B6, E0, B2 If Both SHIFT ON, send E0, B6, E0, AA, E0, 52.	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0,52	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, D2, E0, 2A If Right SHIFT ON, send E0, D2, E0, 36. If Both SHIFT ON, send E0, D2, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 52.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0, 52.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, D2, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 52	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 52.	case (iv) NUM LOCK ON, SHIFT ON, send E0, D2.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Delete	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 53	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,53.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, D3.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 53 If Right SHIFT ON, send E0, B6, E0, 53. If Both SHIFT ON, send E0, B6, E0, AA, E0, 53	case (ii) NUM LOCK OFF' SHIFT ON, repeatly send E0, 53	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, D3, E0, 2A. If Right SHIFT ON, send E0, D3, E0, 36. If Both SHIFT ON, send E0, D3, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 53	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0,53.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, D3, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 53.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0,53.	case (iv) NUM LOCK ON, SHIFT ON, send E0, D3.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Home	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 47	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0, 47.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, C7.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 47 If Right SHIFT ON, send E0, B6, E0, 47 If Both SHIFT ON, send E0, B6, E0, AA, E0, A7	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0, 47	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, C7, E0, 2A. If Right SHIFT ON, send E0, C7, E0, 36. If Both SHIFT ON, send E0, C7, E0, 36, E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 47.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0, 47.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, C7, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 47.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 47.	case (iv) NUM LOCK ON, SHIFT ON, send E0, C7.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
↓	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 50.	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,50.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, D0.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 50. If Right SHIFT ON, send E0,B6, E0,50 If Both SHIFT ON, send E0,B6, E0,AA,E0,50.	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0, 50	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0, D0, E0, 2A. If Right SHIFT ON, send E0, D0, E0,36. If Both SHIFT ON, send E0, D0, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 50.	case (iii) NUM LOCK ON SHIFT OFF, repeatly send E0, 50.	case (iii) NUM LOCK ON SHIFT OFF, send E0, D0, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 50.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0,50.	case (iv) NUM LOCK ON, SHIFT ON, send E0,D0.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
←	case(i) NUM LOCK OFF and SHIFT OFF, send E0, 4B.	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0, 4B.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, CB.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON send E0, AA, E0, 4B. If Right SHIFT ON, send E0, B6, E0, 4B If Both SHIFT ON, send E0, B6, E0, AA, E0, 4B.	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0, 4B	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, CB, E0, 2A. If Right SHIFT ON, send E0, CB, E0, 36. If Both SHIFT ON, send E0, CB, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 4B.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0, 4B.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, CB, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 4B.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0,4B.	case (iv) NUM LOCK ON, SHIFT ON, send E0,CB.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
↑	case (i) NUM LOCK OFF and SHIFT OFF, send E0,48.	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0, 48.	case (i) NUM LOCK OFF and SHIFT OFF, send E0, C8.
	case (ii) NUM LOCK OFF SHIFT ON,' If Left SHIFT ON, send E0,AA, E0,48 If Right SHIFT ON, Send E0, B6,E0,48. If Both SHIFT ON, send E0, B6, E0, AA, E0, 48.	case (ii) NUM LOCK OFF, SHIFT ON,' repeatly send E0, 48.	case (ii) NUM LOCK OFF SHIFT ON,' If Left SHIFT ON, send E0,C8, E0,2A. If Right SHIFT ON, Send E0, C8, E0, 36. If Both SHIFT ON, send E0, C8, E0, 36, E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, Send E0, 2A, E0, 48	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0, 48	case (iii) NUM LOCK ON, SHIFT OFF, Send E0, C8, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 48.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 48	case (iv) NUM LOCK ON, SHIFT ON, send E0, C8

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Page Down	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 51	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,51.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,D1.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 51 If Right SHIFT ON, send E0, B6, E0,51 If Both SHIFT ON, send E0, B6, E0, AA, E0, 51	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0,51	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, D1, E0, 2A. If Right SHIFT ON, send E0, D1, E0, 36. If Both SHIFT ON, send E0,D1,E0,36 E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 51.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0,51.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, D1, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 51.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 51.	case (iv) NUM LOCK ON, SHIFT ON, send E0, D1.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Page Up	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 49	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,49.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,C9.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 49. If Right SHIFT ON, send E0, B6, E0, 49 If Both SHIFT ON, send E0, B6, E0, AA, E0, 49	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0,49	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, C9, E0, 2A. If Right SHIFT ON, send E0, C9, E0, 36. If Both SHIFT ON, send E0, C9, E0, 36 E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 49.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0,49.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, C9, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 49.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0, 49.	case (iv) NUM LOCK ON, SHIFT ON, send E0, C9.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
End	case (i) NUM LOCK OFF and SHIFT OFF, send E0, 4F	case (i) NUM LOCK OFF and SHIFT OFF, repeatly send E0,4F.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,CF.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, AA, E0, 4F If Right SHIFT ON, send E0, B6, E0, 4F If Both SHIFT ON, send E0, B6, E0, AA, E0, 4F.	case (ii) NUM LOCK OFF, SHIFT ON, repeatly send E0,4F	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0, CF, E0, 2A. If Right SHIFT ON, send E0, CF, E0, 36. If Both SHIFT ON send E0,CF,E0,36 E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0, 2A, E0, 4F.	case (iii) NUM LOCK ON, SHIFT OFF, repeatly send E0,4F.	case (iii) NUM LOCK ON, SHIFT OFF, send E0, CF, E0, AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 4F.	case (iv) NUM LOCK ON, SHIFT ON, repeatly send E0,4F.	case (iv) NUM LOCK ON, SHIFT ON, send E0, CF.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
~ `	29	repeatly 29	A9
! 1	02	repeatly 02	82
@ 2	03	repeatly 03	83
# 3	04	repeatly 04	84
$ 4	05	repeatly 05	85
% 5	06	repeatly 06	86
^ 6	07	repeatly 07	87
& 7	08	repeatly 08	88
* 8	09	repeatly 09	89
(9	0A	repeatly 0A	8A
) 0	0B	repeatly 0B	8B
+ =	0D	repeatly 0D	8D
| \	2B	repeatly 2B	AB

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
←	0E	repeatly 0E	8E
Tab ⇤⇥	0F	repeatly 0F	8F
Q	10	repeatly 10	90
W	11	repeatly 11	91
E	12	repeatly 12	92
R	13	repeatly 13	93
T	14	repeatly 14	94
Y	15	repeatly 15	95
U	16	repeatly 16	96
I	17	repeatly 17	97
O	18	repeatly 18	98
P	19	repeatly 19	99
{ [	1A	repeatly 1A	9A

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
}]	1B	repeatly 1B	9B
A	1E	repeatly 1E	9E
S	1F	repeatly 1F	9F
D	20	repeatly 20	A0
F	21	repeatly 21	A1
G	22	repeatly 22	A2
H	23	repeatly 23	A3
J	24	repeatly 24	A4
K	25	repeatly 25	A5
L	26	repeatly 26	A6
: ;	27	repeatly 27	A7
" '	28	repeatly 28	A8

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Z	2C	repeatly 2C	AC
X	2D	repeatly 2D	AD
C	2E	repeatly 2E	AE
V	2F	repeatly 2F	AF
B	30	repeatly 30	B0
N	31	repeatly 31	B1
M	32	repeatly 32	B2
< ,	33	repeatly 33	B3
> .	34	repeatly 34	B4
? /	35	repeatly 35	B5
Space Bar	39	repeatly 39	B9
0 Ins	52	repeatly 52	D2
. Del	53	repeatly 53	D3

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
1 End	4F	repeatly 4F	CF
2 ↓	50	repeatly 50	D0
3 Pg Dn	51	repeatly 51	D1
4 ←	4B	repeatly 4B	CB
5	4C	repeatly 4C	CC
6 →	4D	repeatly 4D	CD
7 Home	47	repeatly 47	C7
8 ↑	48	repeatly 48	C8
9 Pg Up	49	repeatly 49	C9

3.3.3 Keyboard Timing

The typical timing for a single scan code and for a muticode are shown in Fig 3.4 and Fig 3.5 respectively.

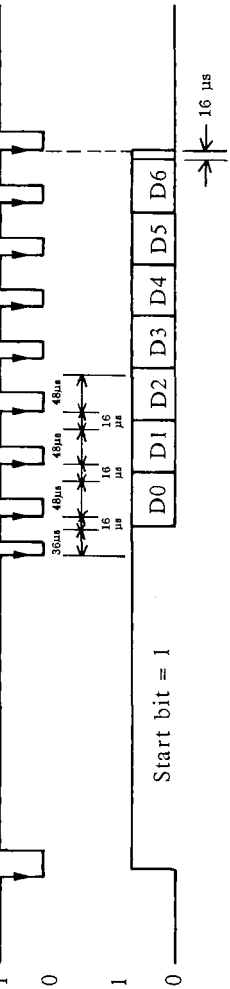


Fig. 3.4 Typical timing for a single scan code

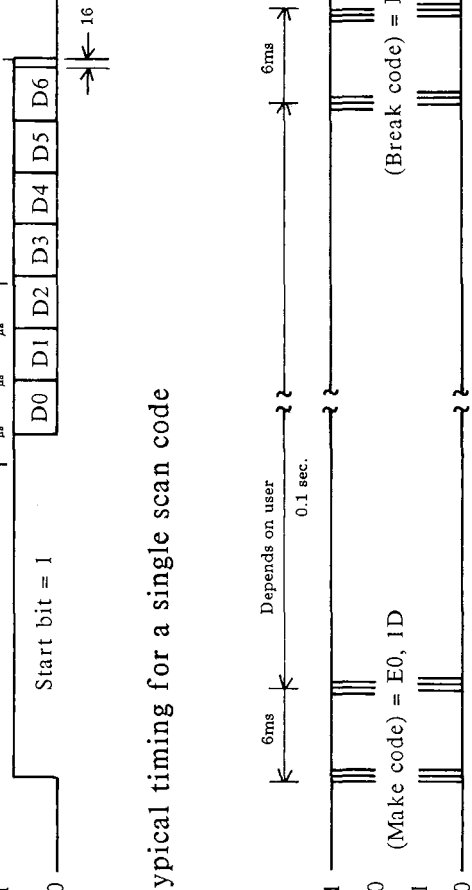
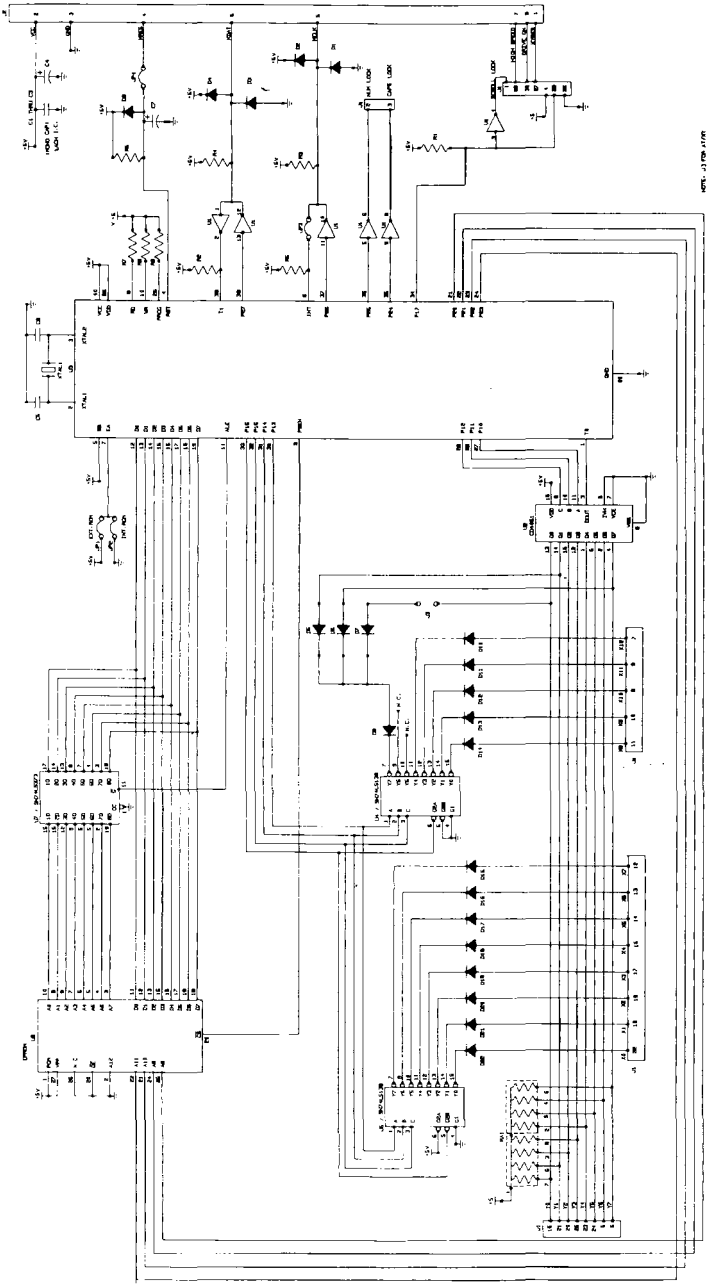
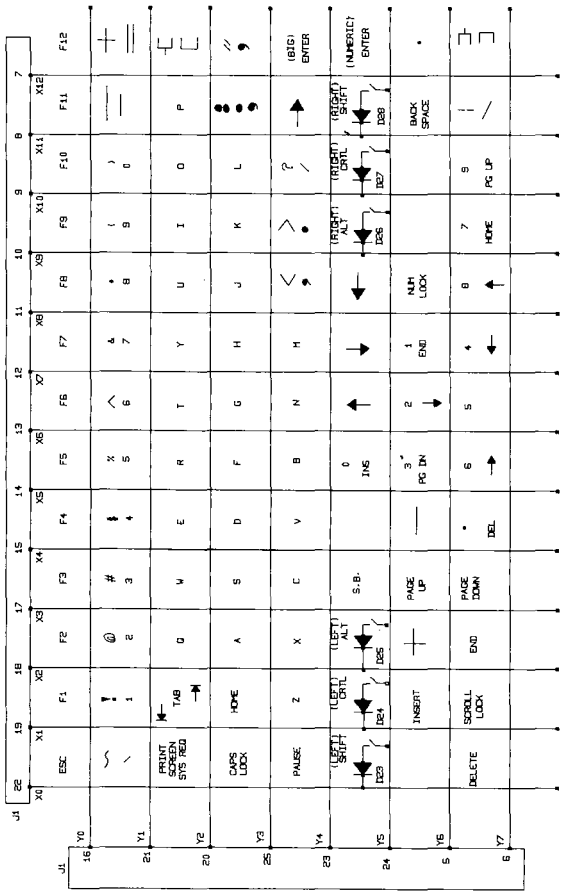


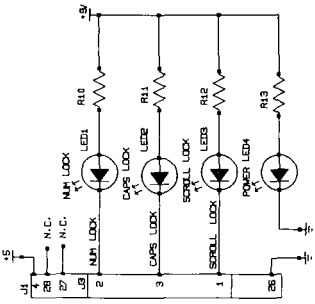
Fig. 3.5 Typical timing for multicode generated consecutively

3.4 Enhanced keyboard interface circuit



3.5 Enhanced keyboard matrix





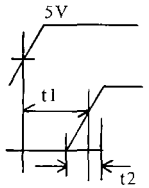
CHAPTER 4

POWER SUPPLY

4. POWER SUPPLY

4.1 Power Supply Specification

Item	Conditions*		Min	Type	Max	Unit
Input Voltage	110V Switched		90	110	132	VAC
	220V Switched		180	220	264	VAC
Input Frequency			47		63	Hz
Loading Range		5V	3		15	A
		12V	1.5		4.2	A
		-5V	0.0		0.3	A
		-12V	0.0		0.3	A
Total Regulation	Overall loading and input ranges	5V			±5%	
		12V			+10%-5%	
		-5V			±15%	
		-12V			±15%	
Noise and Ripple		5V			100	MVp-p
		12V			200	MVp-p
		-5V			100	MVp-p
		-12V			200	MVp-p
Efficienty			70%			
Transient A. Overshoot	1KHz square test wavefrom, switching from min. to max. other rail kept at max. loading	5V			10%	
		12V			10%	
		-5V			10%	
		-12V			10%	
Transient Response B. Settling Time		5V			10	us
		12V			10	us
		-5V			10	us
		-12V			10	us

Item	Conditions*		Min	Type	Max	Unit
Overvoltage Protection Threshold	5V				6.5	V
S/C input Power	Any rail shorted to GND				10	W
Inrush current					60	A
Power good Signal		VOH	3.0			V
		VOL			0.4	V
		IOL			4	MA
		IOH			-1.0	MA
		t1	100			MSec
		t2			5	usec
Hi-Pot Potential	Between Pri-Sec for 1 min. Pri-E		2500 2500			VDC VDC
EMI	Meets FCC class B					
Safety	UL listed E104979					
Mechanical Dimension	Compatible with standard PC XT Switching Power Supply					

*Condition: Normal line
max. load
unless otherwise specified

4.2 Output Connector Pin Out

The power supply connectors and pin assignments is shown in Fig 4.1

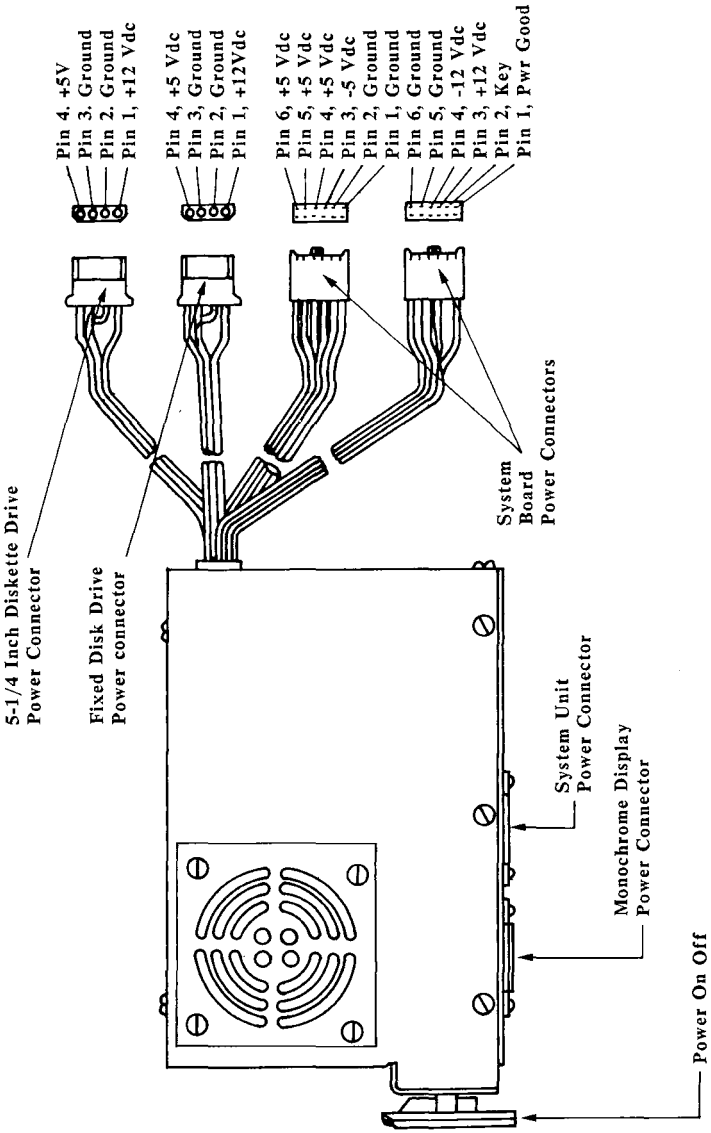


Fig 4.1 Power Supply and connectors

The color of the wire of different pin out is as follow:

Pin Out	Color
+5	red
+12	yellow
-5	white
-12	blue
GND	black
Power good	orange

4.3 Power Consumption

The Power consumption estimation of the LASER Turbo XT is summarized in the following table.

Supply voltage (V)	5	12
Supply current (A)	15	4.2
Current taken by (A) System board	2	-
Current taken by 1st (A) 5" 1/4. drive	0.6	0.9
Current taken by 2st (A) 5" 1/4. drive	0.6	0.9
Current taken by one (A) 20 MB Hard Disk	0.7	1.8
Current available for slots (8 slots) (A)	11.1	0.6
Average current available for each slot (A)	1.38	0.075

CHAPTER 5

SYSTEM BIOS

5. SYSTEM BIOS

5.1 Interrupt Calls Overview

The BIOS routines are called through the 8088 software interrupt. The parameters are passed using the 8088 registers. The following section provides an overview on the various routines.

1. Interrupt Hex 0 - Divide by Zero

2. Interrupt Hex 1 - Single Step

3. Interrupt Hex 2 - Nonmaskable

   When this interrupt is called, the interrupt handler will print a parity error message. The segment addresses will be also be printed.

4. Interrupt Hex 3 - Breakpoint

5. Interrupt Hex 4 - Overflow

6. Interrupt Hex 5 - Print Screen

   This interrupt is used to copy the content of the screen to the printer. The current cursor position will be saved and restored when printing is completed.

7. Interrupt Hex 6 - Reserved

8. Interrupt Hex 7 - Reserved

9. Interrupt Hex 8 - Time of Day

   The interrupt handler handles the timer interrupt from channel 0 of the timer. There are 18.2 interrupts per second. The interrupt handler keeps a count of interrupts since power on time. This can be used as the time of day. The interrupt handler also decrements the motor control count of the diskette, and turn off the diskette motor and reset the motor running flags when the count reach zero.

10. Interrupt Hex 9 - Keyboard

    This interrupt handler handles keyboard interrupt.

11. Interrupt Hex A - Reserved

12. Interrupt Hex B - Communications

13. Interrupt Hex C - Communications

14. Interrupt Hex D - Disk

15. Interrupt Hex E - Diskette

    This interrupt handler handle the diskette interrupt.

16. Interrupt Hex F - Printer

17. Interrupt Hex 10 - Video
    This interrupt provides the CRT interface

18. Interrupt Hex 11 - Equipment check
    This interrupt handler reports the configuration of the system.

19. Interrupt Hex 12 - Memory
    This interrupt handler determines the amount of memory in the system.

20. Interrupt Hex 13 - Diskette Disk
This interrupt provides access to 5" 1/4 diskette drive.

21. Interrupt Hex 14 - Communications
This interrupt handler provides byte stream I/O to the communication ports.

22. Interrupt Hex 15 - Cassette
Dummy cassette I/O routine. Always return the error code "invalid command".

23. Interrupt Hex 16 - Keyboard
This interrupt provides Keyboard support.

24. Interrupt Hex 17 - Printer
This interrupt provides communication with the printer.

25. Interrupt Hex 18 - Resident BASIC

26. Interrupt Hex 19 - Bootstrap

This interrupt handler is the boot strap loader which perform the following procedures.

- The fixed disk BIOS substitutes the interrupt 19 Boot strap vector by a pointer to the boot routine.

- The default disk and diskette parameter vectors is reset.

- The boot block from cylinder 0 sector 1 of the device will be read in.

- The Bootstrap sequence is:
> Try to load from the diskette into the boot location (0000:7C00) and transfer control there
> If the diskette fails, the fixed disk is tried for a valid bootstrap block. A valid boot block on the fixed disk consists of the bytes 055H OAAH as the last two bytes of the block.

27. Interrupt Hex 1A - Time of Day

    This interrupt handler set and read the clock.

28. Interrupt Hex 1B - Keyboard Break

    This interrupt handler will be called when the Ctrl and Break keys on the keyboard are pressed.

29. Interrupt Hex IC - Timer Tick

    This interrupt handler will be called from the timer interrupt service routine.

30. Interrupt Hex 1D - Video Parameters

    This interrupt vector points to a table containing the parameters for initializing the 6845 on the display adaptor.

31. Interrupt Hex IE - Diskette parameter

    This interrupt vector points to a table containing the parameters used by the diskette drive.

32. Interrupt Hex 1F - Graphics Character Extensions.

33. Interrupt Hex 40 - Reserved

    When an Fixed Disk Drive Adapter is installed, this interrupt is used to revector the diskette pointer.

34. Interrupt Hex 41 - Fixed Disk Parameters

    This interrupt vector points to a table containing the parameters used by the fixed disk drive.

5.2 Interrupt call summary

Service	Interrupt (Hex)	Register Input	Output	Description
Print screen	05	AH=05	n/a	Send screen contents to printer. Status and result byte at low-memory address hex 500 (0050:0000)
Video Services				
Set video mode	10	AH=00 AL=Video mode	none	Video modes in AL: 00:40 x 25 text, 16 B/W 01:40 x 25 text, 16/8 color 02:80 x 25 text, 16 B/W 03:80 x 25 text, 16/8 color 04:320 x 200 graphics, 4 color 05:320 x 200 graphics, 4 B/W 06:640 x 200 graphics, B/W 07:80 x 25 text, B/W
Set cursor size	10	AH=01 CH=starting scan line CL=ending scan line	none	Color/Graphics Adapter uses lines 0-7 Monochrome Adapter uses lines 0-13
Set cursor position	10	AH=02 BH=display page number DH=row DL=column	none	
Read cursor position	10	AH=03 BH=display page number	CH=starting scan line Cl=ending scan line DH=row DL=column	
Read light-pen position	10	AH=04	AH=pen trigger signal BX=pixel column CH=pixel row DH=character row DL=character column	
Set active display page	10	AH=05 AL=page number		

Scroll window up	10	AH=06 AL=lines to scroll up BH=filler attribute CH=upper row CL=left column DH=lower row DL=right column	none
Scroll window down	10	AH=07 AL=ines to scroll down BH=filler attribute CH=upper row CL=left column DH=lower row DL=right column	none
Read character and attribute	10	AH=08 BH=display page number	AH=character AL=attribute
Write character and attribute	10	AH=09 AL=character BH=page number BL=attribute CX=number of characters to repeat	none
Write character	10	AH=0A AL=character BH=page number BL=color in graphics mode CX=count of characters	none
Set color palette	10	AH=0B BH=palette color ID BL=color to be used with palette ID	none
Write pixel dot	10	AH=OC AL=color CX=pixel column DL=pixel row	none
Read pixel dot	10	AH=0D CX=pixel column DL=pixel row	AL=color read
Write character	10	AH=0E AL=character BL=color for TTY graphics mode	none
Get current video mode	10	AH=OF	AH=width in characters AL=video mode BH=page number

Equipment-List Service				
Get list of peripheral attached equipment	11	none	AX=equipment list, bit-coded	Bit settings in AX: 00=disk drive 01=math coprocessor 02, 03=system board RAM in 16K blocks 04, 05=initial video mode 00=unused; 01=40 x 25 color; 10=80 x 25 color; 11=80 x 25 B/W 06, 07=number of disk drives 08=DMA present? 00=yes; 01=no 09, 10, 11=number of RS-232 cards in system 12=game I/O attached 13=serial printer attached 14, 15=number of printers attached
Memory Service				
Get usable memory size (in K-bytes)	12	none	AX=memory size	
Diskette Service				
Reset diskette system	13	AH=00	none	
Get diskette status	13	AH=01	AL=Status code	Status values: AL=1:bad command AL=2:address mark not found AL=3:write atempted on write-protected disk AL=4:sector not found AL=6:diskette removed AL=8:DMA overrun AL=9:DMA across 64K boundary AL=10:bad CRC AL=20:NEC controller failed AL=40:seek failure AL=80:time out

Read diskette sectors	13	AH=02 AL=number of sectors CH=track CL=sector number DH=head number DL=drive number ES:BX=pointer to buffer	CF=success/ failure signal AH=status code AL=number of number sectors read	Status codes in AH: see diskette service 01
Write diskette sectors	13	AH=03 AL=number of sectors CH=track CL=sector number DH=head number DL=drive number ES:BX=pointer to buffer	CF=success/ failure flag AH=status code AL=number of sectors written	Status codes in AH: see diskette service 01
Verify diskette sectors	13	AH=04 AL=number of sectors CH=track number CL=sector number DH=head number DL=drive number	CF=success/ failure (signal) AH=status code AL=number of sectors	Status codes in AH: see diskette service 01
Format diskette track	13	AH=05 AL=number of sectors CH=track number CL=sector number DH=head number DL=drive number ES:BX=pointer to list of 4-byte address fields: Byte 1=track Byte 2=head Byte 3=sector Byte 4=bytes/sector	CF=success/ failure signal AH=status code	Status codes in AH: see diskette service 01
Serial Port Services				
Initialize serial port parameters	14	AH=00 DX=serial port number	AX=serial port status	Status bit settings: 00, 01=word length 10=7 bits; 11-8 bits 02=stop bits:0=1;1=2 03, 04=parity: 00, 01=none; 01=odd; 11=even 05, 06, 07= baud rate; 000=110; 001=150; 010=360; 011=600; 100=1,200; 101=2,400; 110=4,800; 111=9,600

Send out one character	14	AH=01 AL=character code DX=serial port number	AH=success/ failure status AL=modem status	AH bit setings: 00=data ready; 01=overrun error; 02=parity error; 03=framing error; 04=break detected; 05=transmission buffer register empty; 06=transmission shift register empty; 07=time out AL bit settings: 00=delta clear-to-send; 01=delta data-set-ready; 02=trailing edge ring detected; 03=change, receive line signal detected 04=clear-to-send; 05=data-set-ready; 06=ring detected; 07=receive line signal detected
Receive one character	14	AH=02 DX=serial port number	AH=success/ failure status code AL=character	Status bit settings: see serial port service 01
Get serial port status	14	AH=03	AX=status code	Status code bit settings: see serial port service 00
Cassette Tape services		Dummy service, alway returns a error code of invalid command.		
Keyboard Services				
Read next keyboard character	16	AH=00	AH=scan code (auxiliary byte) AL=character code (main byte)	
Report whether character ready	16	AH=01	ZF=ready or not signal AH=scan code (auxiliary byte) AL=character code (main byte)	

Get shift status	16	AH=02	AL=shift status bits	Shift status bits: Bit 0=1:right Shift depressed Bit 1=1:left Shift depressed Bit 2=1:Ctrl depressed Bit 3=1:Alt depressed Bit 4=1:Scroll Lock active Bit 5=1:Num Lock active Bit 6=1:Caps Lock active Bit 7=1:Insert state active
Printer Services				
Send one byte to printer	17	AH=00 AL=character	AH=success/ failure Status code	Status bit settings: 0=time out 1=unused 2=unused 3=1:I/O error 4=1:selected 5=1:out of paper 6=1:acknowledge 7=1:not busy
Initial-ize printer	17	AH=01	AH=status code	Status code bit settings: see printer service 00
Get printer status	17	AH=02	AH=status code	Status code bit settings: see printer service 00
Miscellaneous Services				
Switch control to BASIC	18	none	n/a	No return, so no possible output
Reboot computer	19	none	n/a	No return, so no possible output
Time-of-Day Services				
Read the current clock count	1A	AH=00	AL=midnight signal CX=tick count, high portion DX=tick count, low portion	
Set current clock count	1A	AH=01 CX=tick count, high portion DX=tick count, low portion	none	

5.3 Laser Turbo XT BIOS Error Message

BEEPS	DESCRIPTION
1 long + 1 short	Base 64K RAM (00000H-0FFFFH) isn't usable. SOLUTION - Check RAM chips
1 long + 2 short	Video switches wrong for the installed adapter. SOLUTION - Check DIP switches and video selection.
1 long + 5 short	BIOS ROM check sum is incorrect. (Bad EPROM) SOLUTION - Replace BIOS chip.

Display Messages

VIDEO ERROR

BIOS couldn't find the display adapter requested by the DIP switches. BIOS is instead using the adapter it did find.
SOLUTION - Check DIP switches and video card.

KEYBOARD ERROR 0100

Keyboard did not respond. (No interrupt) SOLUTION - Check internal connector on the keyboard.

KEYBOARD ERROR 02XX

Keyboard returned wrong test code xx.
SOLUTION - Replace keyboard.

KEYBOARD ERROR 04XX

Keyboard interrupt would not clear.
SOLUTION - Check Gate Array on Motherboard or replace the keyboard.

MEMORY ADDR ERROR SBBBB, DD

Problem with memory addressing. Possibly unconnected RAM legs or shorted address lines.
SOLUTION - Check the RAM chips (replace one at a time). If BBBB=0000 then the problem was detected on address bits A16-A 19; "S" value (0-9) indicates the lowest segment which failed. If BBBB is non-zero, then the problem was found on address lines A0-A15 of the segment "S". The "DD" tells which data bits were wrong.

MEMORY ERROR SBBBB,DD

Other memory problem. The "S" is the 64K segment (0-9). "BBBB" = the offset where the error was found. "DD" = data error bits.

NOTE: The BIOS will not test memory beyond an error and will reduce memory size to exclude the faulty memory.

If memory size is displayed with a decimal point like this:

SYSTEM MEMORY SIZE = 256.K

Means that DIP switch #1 is on, and memory beyond 256K will always be ignored. SOLUTION - Check DIP switches.

DRIVE A ERROR XX

"XX" is the INT 13 error code. If "XX" = 80 Time out (no interrupt, missing, or bad adapter) "XX"=40 Seek error (track 0 not found, missing drive) "XX"=20 Bad NEC controller chip.
SOLUTION - Check all plugs and cables on drive. Check DIP switches on motherboard. Make sure drive select switch is correct. Replace controller card. Replace disk drive.

CHAPTER 6

EMS DRIVER

6. EMS DRIVER

6.1 PROGRAMS INSIDE THE EMS DRIVER PROGRAM DISKETTE

EMM.SYS - The expanded memory manager driver program
This is the driver program for using the expanded memory. It must be installed before the expanded memory can be used.

ERAMDISK.SYS - the RAM disk driver program for the expanded memory.
This is the driver program for implementing a RAM disk in the expanded memory. The RAM disk has a drive ID which is the first unused drive ID in your computer system. For example, if your system has two floppy disk drives, the drive ID of the RAM disk will be C:. If your system has two floppy disk drives and one hard disk, the drive ID of the RAM disk will be D:. You need not change the setting of the DIP switch in your computer mainboard as you implement a RAM disk.

CRAMDISK.SYS - The RAM disk driver program for the conventional memory.

This RAM disk driver program is similar to ERAMDISK.SYS except that the RAM disk occupies conventional memory. The naming of the RAM disk drive ID is the same as that in ERAMDISK. SYS. If both ERAMDISK.SYS and CRAMDISK.SYS are implemented, they will have separate drive IDs. If the CRAMDISK. SYS is implemented, some application programs (e.g. SYMPHONY) which requires large conventional memory size cannot be run.

6.2 PREPARING A EMS SYSTEM DISKETTE

To prepare a system diskette with the EMS driver programs, copy the three driver programs to a bootable system diskette. To copy the driver programs to your system diskette, put your system diskette in drive A: and the EMS driver program diskette in drive B:. Enter the following command.

COPY B: *.SYS A: <CR>

Before you can use the driver programs, you have to create a CONFIG.SYS file in your system diskette. The function of the CONFIG.SYS file is to load the device driver programs at boot time. You can enter the following commands to create a CONFIG.SYS file.

COPY CON: A: CONFIG.SYS ,CR>
DEVICE = EMM.SYS M3 IO <CR>
DEVICE = ERAMDISK.SYS 512 <CR>
DEVICE = CRAMDISK.SYS 128 <CR>
<F6> <CR>

Remark:
<CR> is the ENTER key and <F6> is the F6 function key. The above CONFIG.SYS file is only an example. The entries M3, IO, 512, 128 are parameters for the device drivers. They may be varied for different system configurations or applications. If a RAM disk for conventional memory is not required, the command line DEVICE=CRAMDISK.SYS can be omitted. The command line DEVICE = EMM.SYS must be entered before DEVICE = ERAMDISK.SYS.

Parameters in the device drivers:

EMM.SYS
Format: DEVICE=EMM.SYS Ma Ib [Ib...]

M is the parameter heading defining the starting frame address of the memory in the EMS card. The 'a' after M represents a number which can be 0 to 7.

M parameter	Starting frame address (in Hex)
M0	C4000
M1	C8000
M2	CC000
M3	D0000
M4	D4000
M5	D8000
M6	DC000
M7	E0000

The M parameter can be defined in any of the above values but you must make sure the address space of the EMS memory does not conflict with the interface card with Read Only Memory (ROM). The EMS card occupies 64K address space starting from the frame address (i.e. if M0 is defined, EMS card occupies address C4000-D3FFF). If your system contains a hard disk controller card which has a interface ROM with address C8000-CFFFF, parameter M0 and M1 should not be used. It is recommended to use parameter M3, since the address space does not have conflict with most common interface card.

I is the parameter heading defining the I/O port address of the EMS card installed. The 'b' after I represents a number which can be 0 to 6.

I parameter	I/O port address of EMS board (in Hex)	EMS 1	DIP 2	Switch 3
I0	208	OFF	ON	ON
I1	218	ON	OFF	ON
I2	258	OFF	OFF	ON
I3	268	ON	ON	OFF
I4	2A8	OFF	ON	OFF
I5	2B8	ON	OFF	OFF
I6	2E8	OFF	OFF	OFF

You should define the I parameter according to the DIP switch setting. If your computer system has installed more than one EMS cards (when you fill up more than 2 banks of RAM, you should configure the expanded memory as two cards), the DIP switch setting on each EMS card must be different. You should define one I parameter for one EMS card, two I parameters for two EMS cards installed and so forth. For example, if you have four EMS cards installed, you can define the parameters as follows.

DEVICE=EMM.SYS M3 I0 I1 I2 I3

ERAMDISK.SYS
Format: DEVICE=ERAMDISK.SYS nnnn

nnnn represents a number which defines the RAM disk size in Kbyte of memory. The minimum number is 16 and the maximum number depends on the expanded memory size in your system. If four banks are fully filled with RAM, there are a total of 1024 Kbyte of expanded memory. If these are still not enough for your uses, you can purchase our Expanded Memory card which allows expansion to a maximum of 2 Mbyte per card. (Note: If your system diskette is MSDOS version 2.0 or 2.1 the RAM disk size cannot be defined more than 2048. If your system diskette is MSDOS version 3.0, 3.1, 3.2 or later version, the RAM disk size can be defined up to 8192.

CRAMDISK.SYS
Format: DEVICE=CRAMDISK.SYS nnn

nnn represent a number which defines the RAM disk size in Kbyte of memory. The minimum number is 16 and the maximum number depends on the available conventional memory size. If your application program requires large memory size, it is not recommended to implement this RAM disk.

6.3 PROGRAMMING THE EXPANDED MEMORY

6.3.1 PROGRAMMING GUIDELINE

When using the expanded memory, the programmer should assumes the following:

- There will be more than one expanded memory board.
- Other resident programs may also use expanded memory.

- Program cannot rely on the value of certain register after a function call.

- The size of each page is 16K bytes.

- Four 16K-byte pages can be mapped into a 64K byte region. The starting address of this 64K region is returned by EMM function 2. The 64K bytes region is called page frame.

- The stack should not be located in the expanded memory.

- Since the EMM uses INT 67H, other programs should not use this interrupt vector.

- After testing the presence of the EMM, the page frame base address should be requested.

- The number of free 16K-byte page should be requested so that the maximum number of pages the program can allocated can be determined.

- The EMM functions provide a set of standard expanded memory functions. Programs that deal directly with the hardware or that don't adhere to the specification will have compatibility problem.

6.3.2 Checking the Presence of EMM

There are two methods to check the presence of EMM.

- Issue an open request (MS-DOS function 3DH) using the name of the EMM driver "EMMXXXX0". If the request is successful, issue an 'I/O control for device' command (MS-DOS function 44H) with a 'get device information' command. If the status returned in register AL is 0FFH, then the driver is present. After that, a 'close file handle' command (MS-DOS function 3EH) should be issued to close the EMM device driver.

- Use the INT67H vector to check the device header. If the EMM is present, at offset 0AH of the header will have the string EMMXXXX0. This method must be use if the called program is a device driver or it interrupt DOS during file system operation.

6.3.3 EMM Functions

After ensuring that the Expanded Memory Manager (EMM) is present, an application program communicates with the EMM directly via a software interrupt. The calling sequence for the EMM is:

```
mov   ah, function      ; AH contains the function
                        ;   number
                        ; other registers are loaded
                        ;   with
                        ; function-specific
                        ;   arguments.

int   67h               ; transfer to Expanded
                        ;   Memory Manager.
```

If an EMM call is successful, the value zero is returned in register AH; otherwise, AH will contain an error code.

Int 67H
EMS Function 01H
Get status

Tests whether the EMM and expanded memory hardware is working properly.

INPUT	AH	=	40H	
OUTPUT	AH	=	status	
			00H	*function successful*
			80H	*internal error in EMM software*
			81H	*malfunction in expanded memory hardware*
			84H	*function requested by application not defined*

Int 67H
EMS Function 02H
Get page frame segment

Get the segment address of the page frame used by the EMM

INPUT	AH	=	41H
OUTPUT	If ok		
	AH	=	00H
	BX	=	segment of the page frame

If failed:

AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
84H	*function requested by application not defined*

Int 67H
EMS Function 03H
Get unallocated page count

Get the total number of pages present in the system, and the number of those pages that are free.

Input AH = 42H

OUTPUT If ok

AH = 00H
BX = unallocated pages
DX = total number of pages in the system

If failed:

AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
84H	*function requested by application not defined*

Int 67H
EMS Function 04H
Allocate Pages

Request the EMM for using the expanded memory, obtains a handle and has a certain number of logical pages allocated under the control of this handle.

INPUT AH = 43H
BX = number of logical pages to allocate

OUTPUT If OK
AH = 00H
DX = handle

If failed:
AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
84H	*function requested by application not defined*
85H	*no more handles available*
87H	*allocation request specified more logical pages than are physically available in system; no pages allocated*

88H	*allocation request specified more logical pages than are currently available in system (request does not exceed physical pages that exist, but some are already allocated to other handles); no pages allocated*
89H	*Zero pages requested*

Int 67H
EMS Function 05H
Map Handle page

Maps logical pages of expanded memory assigned to a handle onto one of the four physical pages.

INPUT	AH	=	44H	
	AL	=	physical-page number (0-3)	
	BX	=	logical-page number	
	DX	=	handle	
OUTPUT	AH	=	status	
			00H	*function successful*
			80H	*internal error in EMM software*
			81H	*malfunction in expanded memory hardware*
			83H	*invalid handle*
			84H	*function requested by application not defined*

8AH	*logical page requested to be mapped is outside range of logical pages assigned to handle*
8BH	*illegal physical-page number in mapping request (not in range 0-3)*

Int 67H
EMS Function 06H
Deallocate Pages

Deallocates the logical pages of expanded memory currently allocated to a handle.

INPUT AH = 45H
DX = EMM handle

OUTPUT AH = status

00H	*function successful*
80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
83H	*invalid handle*
84H	*function requested by application not defined*
86H	*error in save or restore of mapping context*

Int 67H
EMS Function 07H
Get EMM version

Returns the version number of the EMM software.

INPUT AH = 46H

OUTPUT If OK

AH = 00H
AL = EMM version number in BCD format. The upper four bits contain the integer digit. The lower four bits contain the fractional digit.

If failed:
AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
84H	*function requested by application not defined*

Int 67H
EMS Function 08H
Save Map

Save the contents of the expanded memory page-mapping registers on the expanded memory boards, which belong to a EMM handle.

INPUT AH = 47H
DX = handle

OUTPUT	AH	=	status
			00H *function successful*
			80H *internal error in EMM software*
			81H *malfunction in expanded memory hardware*
			83H *invalid handle*
			84H *function requested by application not defined*
			8CH *page-mapping hardware state save area is full*
			8DH *save of mapping context failed, save area already contains context associated with requested handle*

Int 67H
EMS Function 09H
Restore page map

Restores the contents of all expanded memory hardware page-mapping registers to the values for particular handle.

INPUT	AH	=	48H
	DX	=	EMM handle

OUTPUT	AH	=	status
			00H *function successful*
			80H *internal error in EMM software*
			81H *malfunction in expanded memory hardware*
			83H *invalid handle*
			84H *function requested by application not defined*
			8EH *restore of mapping context failed; save area does not contain context for requested handle.*

Int 67H
EMS Function 0AH
Reserved

Int 67H
EMS Function 0BH
Reserved

Int 67H
EMS Function 0CH
Get Handle count

Gets the number of active EMM handles.

INPUT AH = 4bh

OUTPUT If OK
AH = 00h
BX = number of EMM handles

If failed:
AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
83H	*invalid handle*
84H	*function requested by application not defined*

Int 67H
EMS Function 0DH
Get EMM Handle Pages

Returns the number of logical expanded memory pages allocated to a specific EMM handle.

INPUT AH = 4CH
DX = EMM handle

OUTPUT If OK
AH = 00H
BX = number of logical pages

If failed:
AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
83H	*invalid handle*
84H	*function requested by application not defined.*

Int 67H
EMS Function 0EH
Get All EMM Handle Pages

Returns an array of all the active handles and the number of logical expanded memory pages allocated to each handle.

INPUT AH = 4DH
ES:DI = segment:offset of array to receive information

OUTPUT If OK

AH = 00h

BX = number of active EMM handles. Each entry in the array is composed of two words, the first contains the EMM handle while the second contains the number of pages allocated to that handle.

If failed:

AH = error code

80H	*internal error in EMM software*
81H	*malfunction in expanded memory hardware*
84H	*function requested by application not defined*

Int 67H
EMS Function 0FH
Get / Set Page Map

Saves or sets the contents of the EMS page-mapping registers on the expanded memory boards.

INPUT AH = 4EH

AL = 00H *if getting mapping registers into array*

01H *if setting mapping registers from array*

02H *if getting and setting mapping registers in one operation*

03H *if returning size of page-mapping array*

DS:SI = *segment:offset of array holding information (subfunction 01H, 02H)*

ES:DI = *segment:offset of array to receive information (subfunction 00H, 02H)*

OUTPUT If OK

AH = 00H

AL = bytes in page-mapping array (subfunction 03H only)

Array pointed to by ES:DI receives mapping information (subfunctions 00H and 02H)

If failed:

AH = error code

80H *internal error in EMM software*

81H *malfunction in expanded memory hardware*

84H *function requested by application not defined*

8FH *subfunction parameter not defined*

CHAPTER 7

SERVICING

7. SERVICING

7.1 Circuit Description

7.1.1 Oscillator Circuit

Various system timing signals are generated by two crystal oscillators. The circuit of the oscillators are shown in Fig 7.1

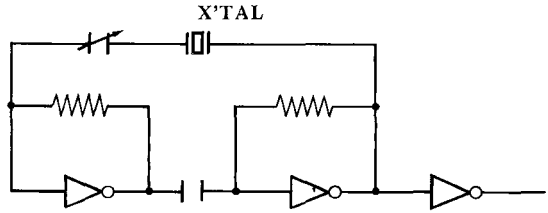


Fig 7.1 Schematic diagram of the crystal oscillator

7.1.2 CPU & Buffers

The 8088-1 CPU is a 8-bit data bus and 16-bit internal architecture microprocessor builds on HMOS technology. The CPU can be run at a clock frequency of 10MHz with 33% duty cycle, this signal is obtained from Gate Array A1. Fig 7.2 shows the interface to the 8088-1 CPU.

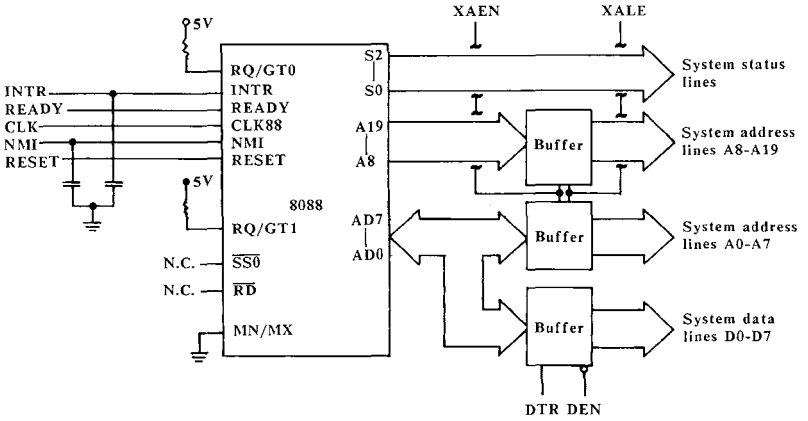


Fig 7.2 Interface to 8088-1 CPU

7.1.3 ROM

On the PCB, there is two sockets for installing ROMs, which is situated at the left middle of the PCB. The leftmost is for installing BIOS using 2764, the other one is for installing BASIC ROM using 27256. Fig 7.3 shows the schematic circuit diagram of ROM.

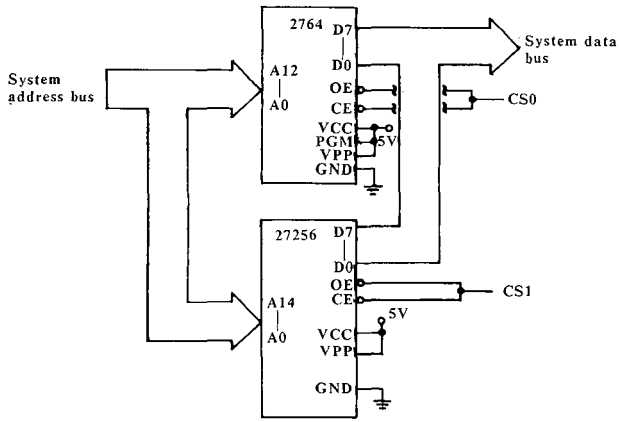


Fig 7.3 Schematic circuit diagram of ROM.

The timing diagram of the ROM 2764 and 27256 is shown in Fig 7.4 and Fig 7.5 respectively.

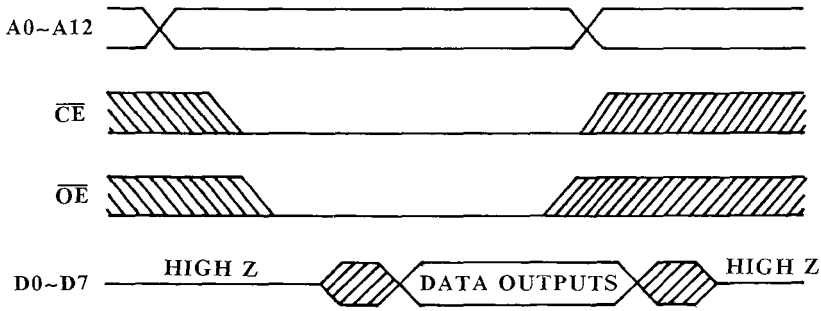


Fig 7.4 Timing diagram of 2764 ROM read

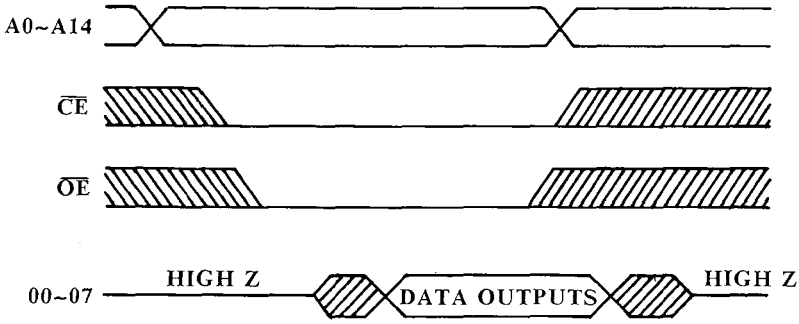


Fig 7.5 Timing diagram of 27256 ROM read

7.1.4 RAM

The computer can supports a maximum of 640K conventional memory and 1M expanded memory.

The 640K conventional memory have four rows of DRAM, the first two rows consists of two 4464 and one 4164. The second two rows consists of nine 41256. The Expanded Memory should be installed with 41256. The RAMs are accessed by the RAS and CAS signals which are obtained from the Gate Array A2.

7.1.5 Speaker circuit

The speaker should be connected to jumper J11. The Speaker circuit is shown in Fig 7.6.

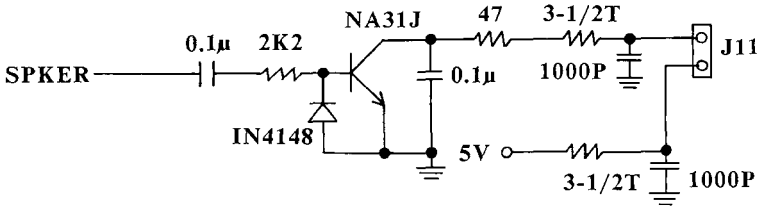


Fig 7.6 Speaker Circuit

7.1.6 Keyboard Lock and LED indicator

Jumper J12 is used for connecting Keyboard Lock, power indicator and High Speed indicator, the jumper should be connected as shown in Fig 7.7.

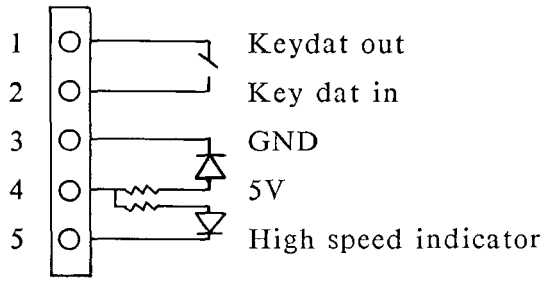
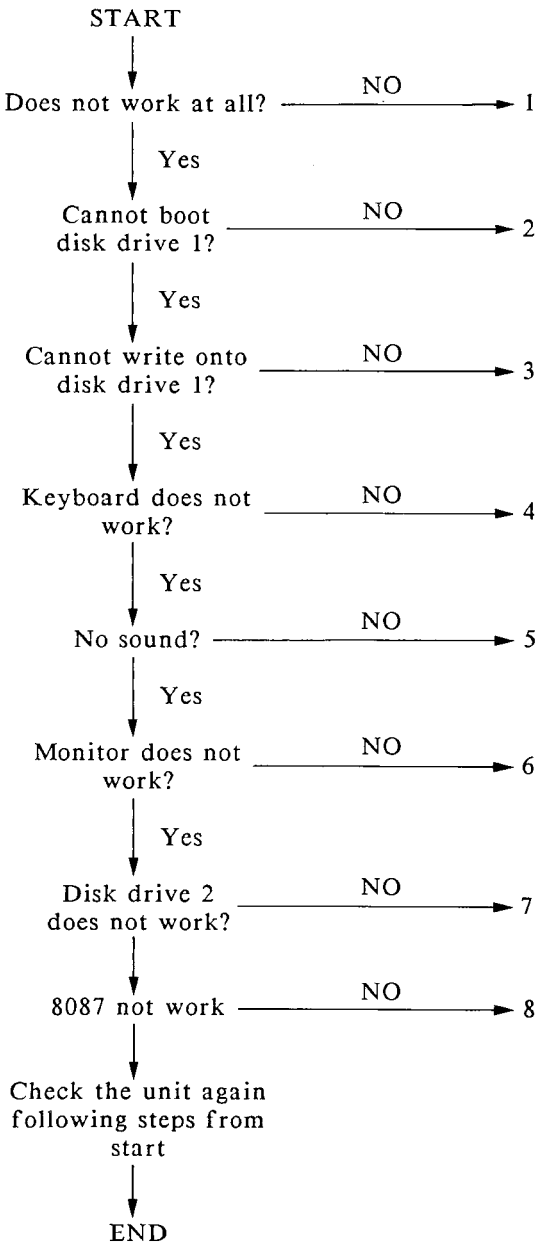
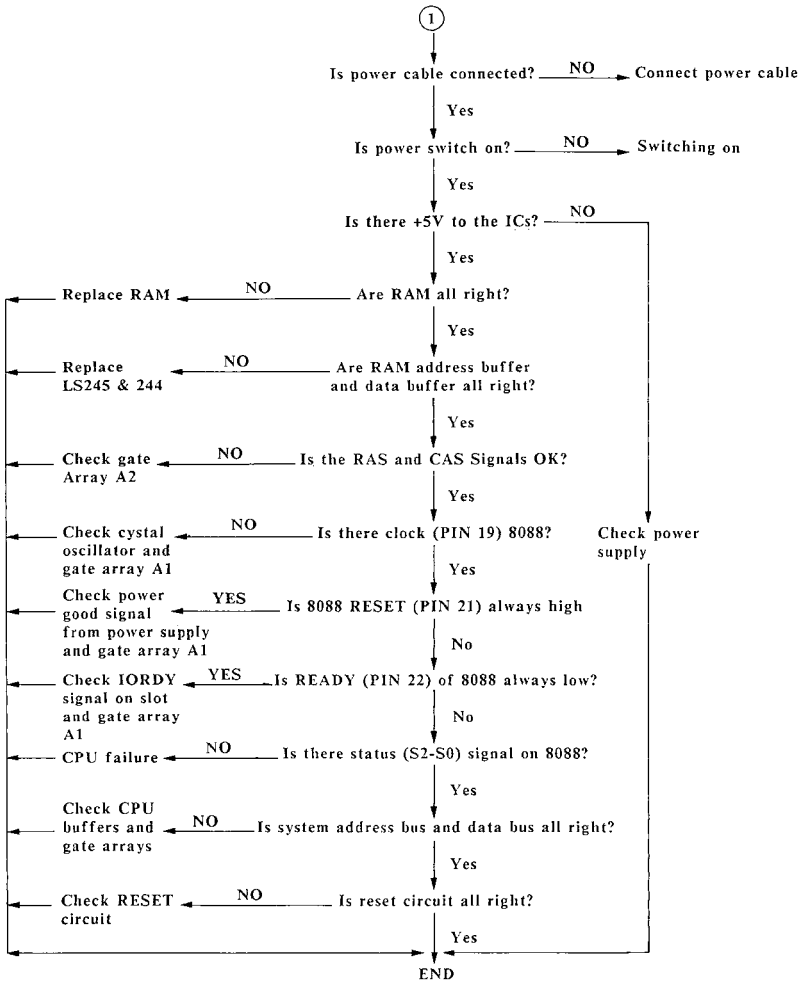
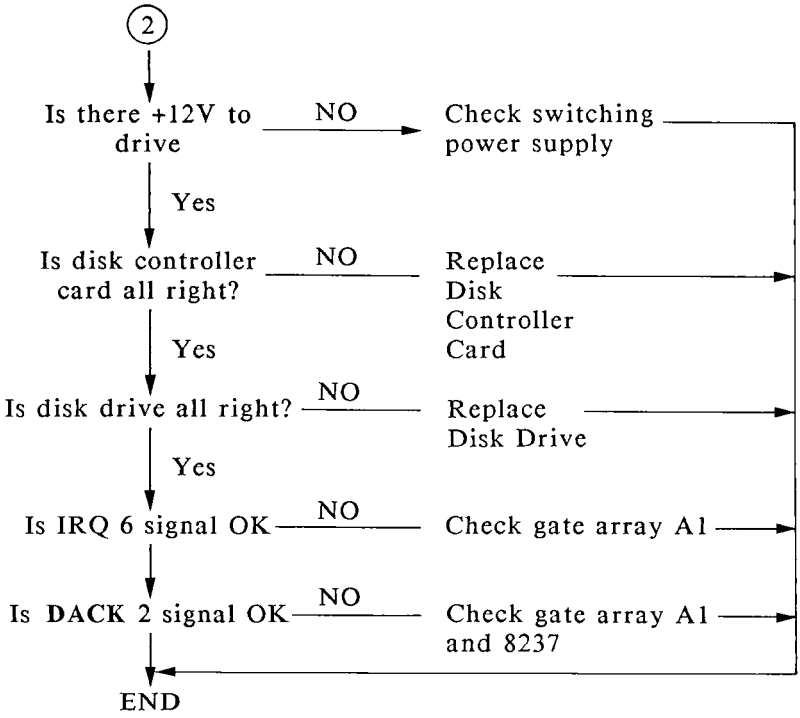


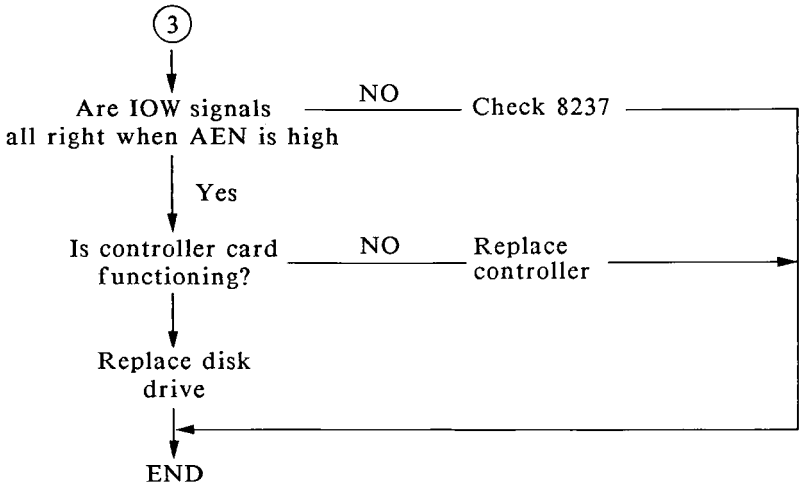
Fig 7.7 circuit of display panel

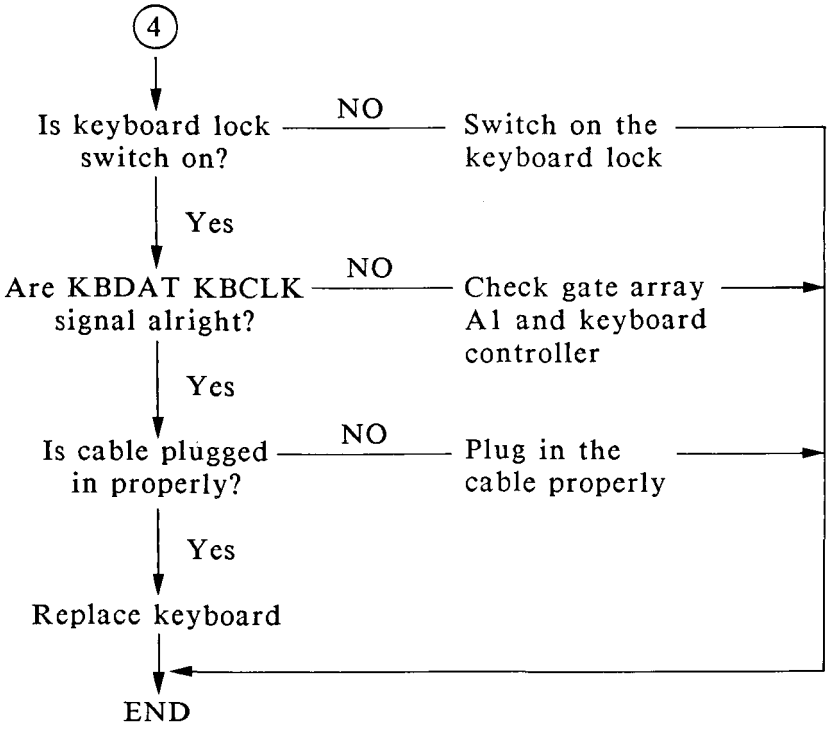
7.2 Service flow Chart

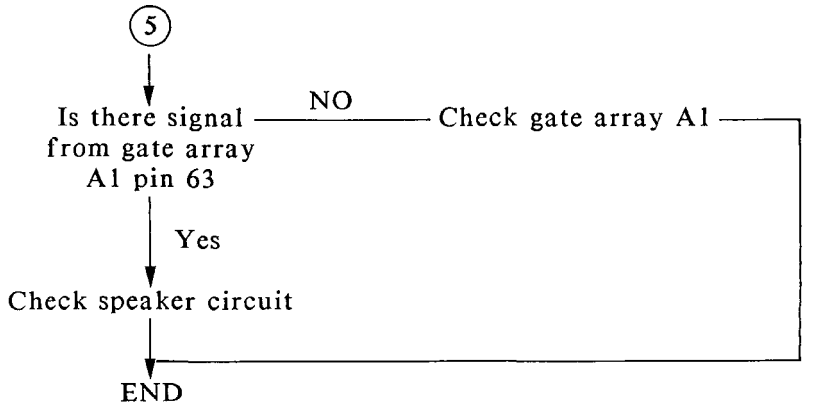


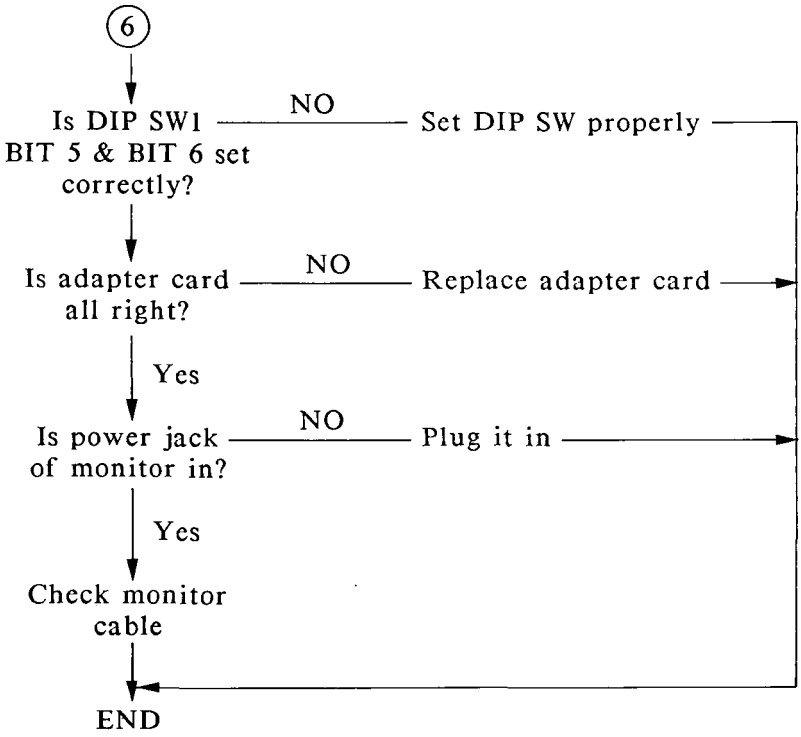

1
Is power cable connected?
NO
Connect power cable
Yes
Is power switch on?
NO
Switching on
Yes
Is there +5V to the ICs?
NO
Yes
Are RAM all right?
NO
Replace RAM
Yes
Are RAM address buffer and data buffer all right?
NO
Replace LS245 & 244
Yes
Is the RAS and CAS Signals OK?
NO
Check gate Array A2
Yes
Is there clock (PIN 19) 8088?
NO
Check cystal oscillator and gate array A1
Check power supply
Yes
Is 8088 RESET (PIN 21) always high
YES
Check power good signal from power supply and gate array A1
No
Is READY (PIN 22) of 8088 always low?
YES
Check IORDY signal on slot and gate array A1
No
Is there status (S2-S0) signal on 8088?
NO
CPU failure
Yes
Is system address bus and data bus all right?
NO
Check CPU buffers and gate arrays
Yes
Is reset circuit all right?
NO
Check RESET circuit
Yes
END

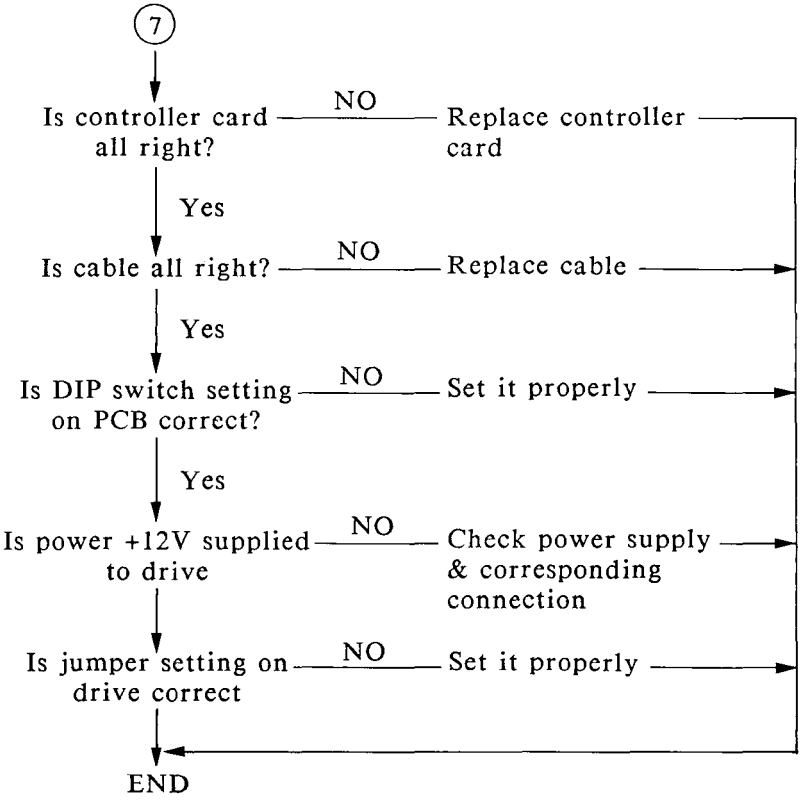

2
Is there +12V to drive
NO
Check switching power supply
Yes
Is disk controller card all right?
NO
Replace Disk Controller Card
Yes
Is disk drive all right?
NO
Replace Disk Drive
Yes
Is IRQ 6 signal OK
NO
Check gate array A1
Is DACK 2 signal OK
NO
Check gate array A1 and 8237
END

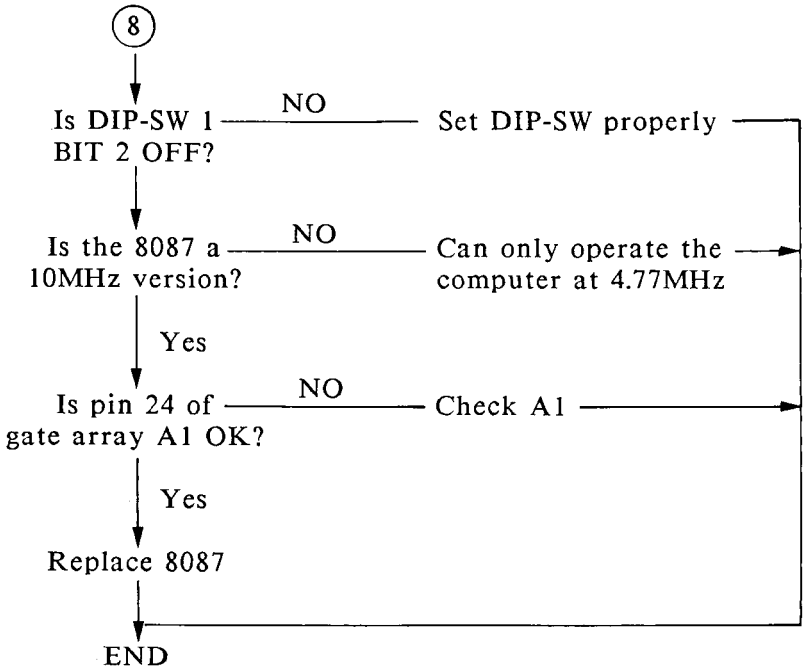

3
Are IOW signals all right when AEN is high
NO
Check 8237
Yes
Is controller card functioning?
NO
Replace controller
Replace disk drive
END


4
Is keyboard lock switch on?
NO
Switch on the keyboard lock
Yes
Are KBDAT KBCLK signal alright?
NO
Check gate array A1 and keyboard controller
Yes
Is cable plugged in properly?
NO
Plug in the cable properly
Yes
Replace keyboard
END


5
Is there signal from gate array A1 pin 63
NO
Check gate array A1
Yes
Check speaker circuit
END


6
Is DIP SW1 BIT 5 & BIT 6 set correctly?
NO
Set DIP SW properly
Is adapter card all right?
NO
Replace adapter card
Yes
Is power jack of monitor in?
NO
Plug it in
Yes
Check monitor cable
END


7
Is controller card all right?
NO
Replace controller card
Yes
Is cable all right?
NO
Replace cable
Yes
Is DIP switch setting on PCB correct?
NO
Set it properly
Yes
Is power +12V supplied to drive
NO
Check power supply & corresponding connection
Is jumper setting on drive correct
NO
Set it properly
END


8
Is DIP-SW 1 BIT 2 OFF?
NO
Set DIP-SW properly
Is the 8087 a 10MHz version?
NO
Can only operate the computer at 4.77MHz
Yes
Is pin 24 of gate array A1 OK?
NO
Check A1
Yes
Replace 8087
END

APPENDIX A

GATE ARRAY
A1 SPECIFICATION

APPENDIX A
GATE ARRAY A1 SPECIFICATION

A.1 A1 Functional Description

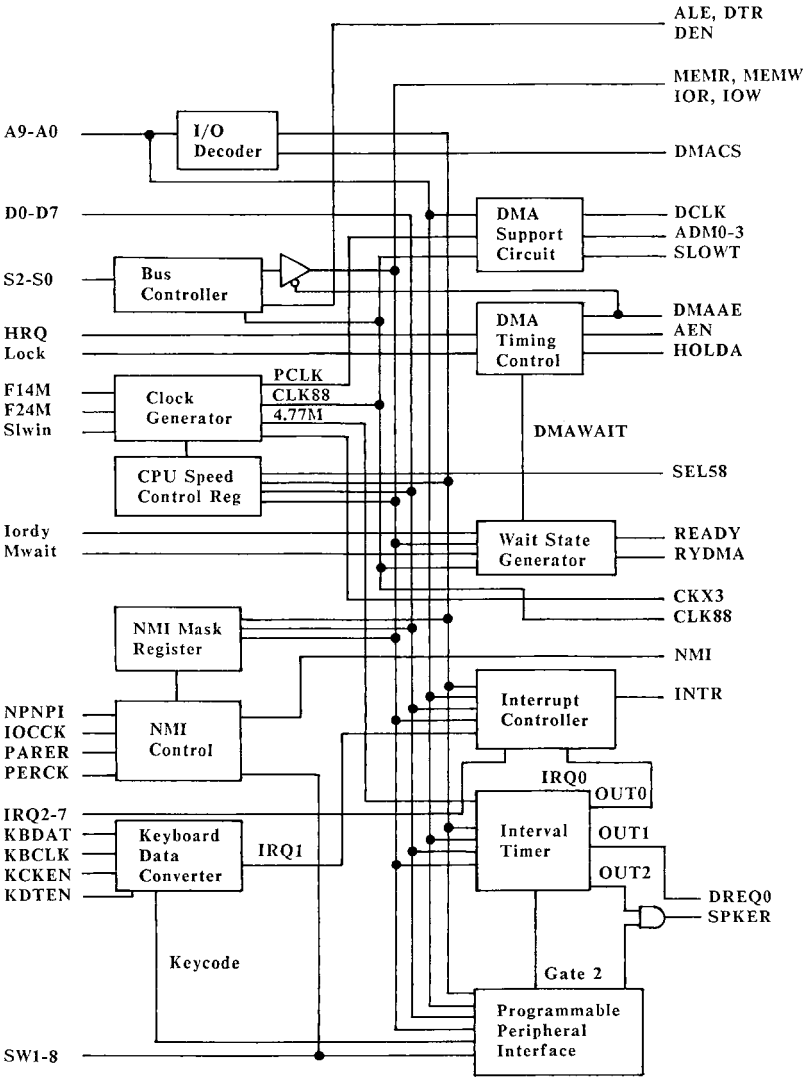
The gate array A1 is used to replaced most of the IBM® PC/XT main board logics. It integrates the functions of the following chips:

- 8284A clock generator
- 8288 bus controller
- 8259A programmable interrupt controller
- 8253-5 programmable interval timer
- 8255A-5 programmable peripheral interface

In addition, it also incorporates the keyboard data converter, the wait state generator, DMA timing generator and I/O decoding circuitry.

The gate array A1 was designed to support high speed operation of the microprocessor. The processor can be switched to operate at the standard speed (4.77MHz) or higher speed through the control of software.

A.2 A1 FUNCTION DIAGRAM



A.3 Gate Array A1 Pin Usage

Pin No	Pin type	Name	Description
2	I	A9	CPU address line
3	I	A8	"
4	I	A7	"
5	I	A6	"
6	I	A5	"
7	I	A4	"
8	I	A3	"
9	I	A2	"
10	I	A1	"
11	I	A0	"
28	I/O	D7	CPU data line
29	I/O	D6	"
30	I/O	D5	"
31	I/O	D4	"
32	I/O	D3	"
33	I/O	D2	"
34	I/O	D1	"
35	I/O	D0	"

12	I	S2	Status Inputs from CPU.
13	I	S1	External pull up needed.
14	I	S0	

S2	S1	S0	Signal activated
0	0	0	INTA (internal signal)
0	0	1	IOR
0	1	0	IOW
0	1	1	halt (no signal active)
1	0	0	MEMR
1	0	1	MEMR
1	1	0	MEMW
1	1	1	no signal active

16	I	LOCK	Lock signal from CPU. Disable DMA operation when low.
17	I	F14M	14.31818 MHz clock input. It is divided by 3 to obtain the CPU clock at standard speed.
18	I	F24M	High frequency clock input. It is divided by 3 to obtain the CPU clock at high speed.
77	O	CKX3	Three times the frequency of CLK88. Always synchronizes with CLK88.
19	O	CLK88	Clock for the CPU. 33% duty cycle. 4.77 M at standard speed. At high speed mode equals to F24M divided by 3.

21	O	ALE	Address latch enable. (active high) This signal is used to strobe an address into the address latches during T1.
22	O	DEN	Data Enable. (active low, the corresponding signal of 8288 is active high) It is used to enable data onto either the local or system data bus.
23	O	DTR	Data Transmit/Receive It establishes the direction of data flow through the transceivers. A high indicates Transmit and a low indicates Receive.
39	I/O	MEMW	Memory Write, active low
40	I/O	MEMR	Memory Read, active low
42	I/O	IOW	I/O Write, active low
43	I/O	IOR	I/O read, active low These four signals will be tristated during DMA operation. During which these signals are asserted by the DMA controller. External pull up are needed.
26	O	READY	Ready signal to CPU. It is used to insert wait states to the CPU.

62	I	MWAIT	Memory Wait It serves to insert wait state to the CPU during memory read or write operation. A wait state is only insert under the following conditions: - the system is in high speed mode - MWAIT is high MWAIT must be stable throughout the period when MEMR or MEMW is active.
27	O	INTR	Interrupt Request to CPU
25	O	NMI	Non-maskable Interrupt request to CPU
24	I	NPNPI	Interrupt Request from the numeric processor. When this signal is active (high), a NMI will be initiated if the signal SW2 is also high.
44 45 46 47 48 38	I I I I I I	IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2	Interrupt requests from peripherals. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the CPU. These lines are pulled low internally.
1	I	IOCHK	I/O Channel Check When this input is low, a NMI will be initiated to the CPU.

37	I	IORDY	I/O Channel Ready This line, normally high (ready), is pulled low to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting a valid address and a Read or Write command.
60	I	EXRES	Active low reset input. Serves for power up reset. Internal Schmitt trigger input.
100	I	KYRES	Active low reset input. Serves for external hardware reset. Internal Schmitt trigger input.
49	O	SYRES	Active low reset output. It is sychronized with the falling edge of CLK88.
50	I	SW8	DIP Switch bit 8
51	I	SW7	DIP Switch bit 7
52	I	SW6	DIP Switch bit 6
53	I	SW5	DIP Switch bit 5
54	I	SW2	DIP Switch bit 2
55	I	SW1	DIP Switch bit 1
56	I/O	KBDAT	Keyboard data input. It will be forced low after receiving an keyboard code.

57	I/O	KBCLK	Keyboard clock The keyboard data is strobed using the falling edge of the keyboard clock. Can be forced low through control of an internal register.
59	O	KDTEN	Keyboard data output enable A low indicates the KBDAT signal is in output mode.
58	O	KCKEN	Keyboard clock output enable. A low indicates the KBCLK signal is in output mode. Both KDTEN and KCKEN is used to control external buffers for the KBDAT and KBCLK signals when the loading is too high, otherwise they can be left unused.
61	I	PARER	Parity error input This is used to detect parity error of RAM. This pin should be tied to the PARER pin of gate array A2. If parity check is not needed, tied this pin to ground.
94	I	PERCK	Parity error clock This is used to strobe the PARER signal. Normally this pin should be tied to the MEMR signal.
66	O	DMACS	DMA controller chip select. active through the address range 000H-01FH.
67	O	RYDMA	Ready signal to the DMA controller

68	O	DCLK	Clock output to the DMA controller
70	O	HOLDA	Hold acknowledge to the DMA controller. It is an active high signal indicating that the CPU has relinquished control of the bus.
71	I	HRQ	Hold Request from the DMA controller.
20	O	AEN	Address Enable When this line is active (high), the DMA controller has control of the address bus, data bus and read write command lines (IOR, IOW, MEMR, MEMW).
96	O	DMAAE	DMA address enable Active (low) during DMA operation. It serves to control address buffers of the DMA controller.
95	I	DACK0	DMA acknowledge 0
72	O	DREQ0	DMA request to the DMA controller channel 0. It is an active high signal which originates from channel 1 of the internal programmable interval timer. This signal is cleared when DACK0 is low. Normally DMA channel 0 serves the function of Dynamic RAM refreshing.
73	OZ	ADM0	To A0 of DMA controller.
74	OZ	ADM1	To A1 of DMA controller.

75	OZ	ADM2	To A2 of DMA controller.
76	OZ	ADM3	To A3 of DMA controller. ADM0 - ADM3 will be tri-stated during DMA operation.
36	O	DIR	Direction control of external data buffer. For large system, the D7 - D0 needed be buffered by external transreceiver. When DIR is low, data is transferred from the A1 to external.
64	I	DCNT1	Data buffer control 1 If the data transreceiver is shared by the DMA controller, tied this pin to DMACS, otherwise to Vcc
79	I	DCNT2	Data buffer control 2 If the data transreceiver is shared by ROM 0, tied this pin to the CS0 signal of gate array A2, otherwise to Vcc
80	I	DCNT3	Data buffer control 3 If the data transreceiver is shared by ROM 1, tied this pin to the CS1 signal of gate array A2, otherwise to Vcc.
97	I	SLWIN	CPU speed select A high selects standard speed (CLK88 = 4.77MHz), a low selects high speed (CLK88 = F24M / 3). Normally this pin should be tied to SLWOT.

98	O	SLWOT	CPU speed control It serves to control the speed of the CPU. This signal will be low when switched to high speed mode. However, it will be forced high under the following condition: - when CPU is doing I/O operation. - when the system is doing DMA operation.
99	O	SEL58	CPU speed indication A high indicates high speed mode. A low indicates standard speed mode.
63	O	SPKER	Speaker output This signal should be connected to a driver circuit to sound a loudspeaker.
81	I	FRSTP	
82	I	RWSEK	
83	I	TRKO	
85	O	STEP	equals to FRSTP AND RWSEK
86	O	FTRK0	equals to RWSEK AND TRK0
78	I	VC0	
84	I	SEPDA	
87	O	RDDAT	equals to VC0 AND NOT SEPDA
88	I	BUFEN	
89	I	RTCEN	
90	I	COMEN	

92	I	GRDEN	
93	O	PDIR	equals to (IOR AND IOW) OR (BUFEN AND RTCEN AND NOT COMEN AND GRDEN) This pins are garbage collector for peripherals. For normal design just tie the inputs to ground and left the outputs unused.
69	I	TEST	Test pin. Must tie it to ground.
15			GROUND
65			GROUND
41			Vcc
91			Vcc

A.4 GATE ARRAY A1 AC CHARACTERISTICS

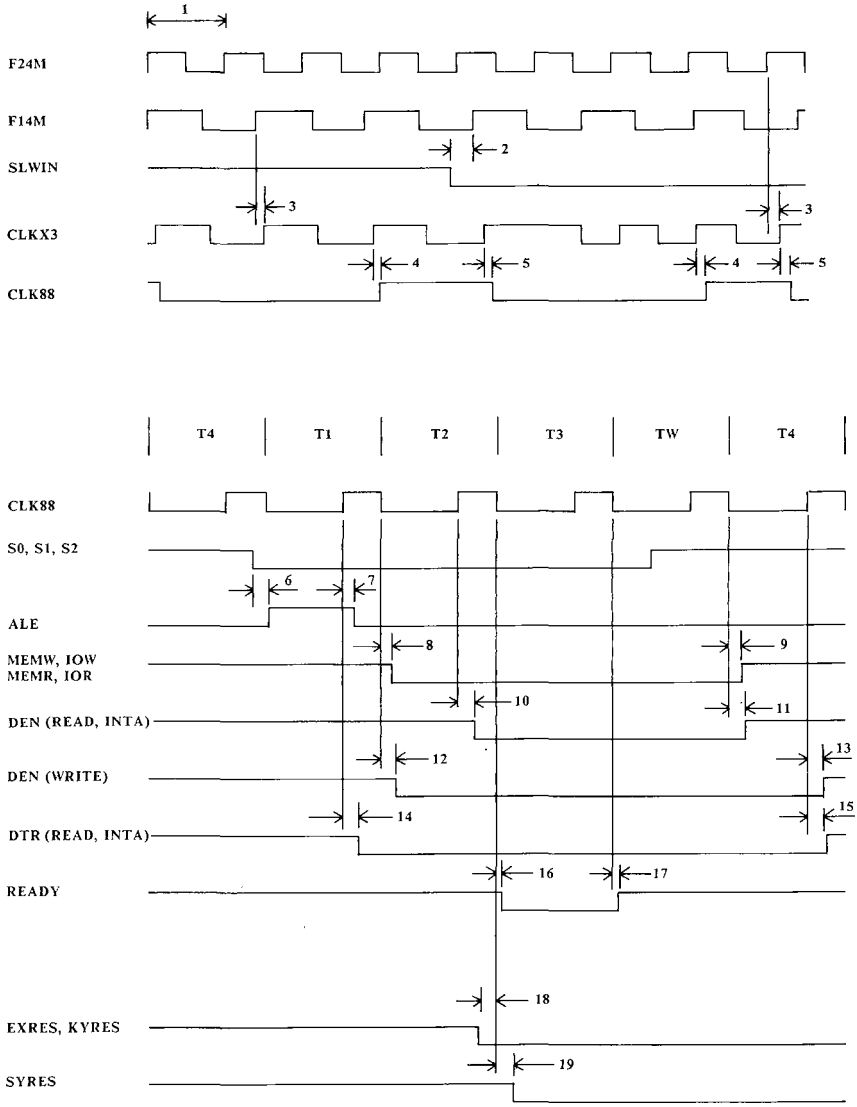
(Vcc = 5V +/-5%, Ta = 0 to 70 C, pin capacitive load = 50pF)

	Min. (ns)	Max (ns)
1. F24M period	27	
2. SLWIN set up time	10	
3. CLKX3 delay from F14M	9	44
4. CLK88 high from CLKX3	6	16
5. CLK88 low from CLKX3	7	20
6. ALE active from S0,S1,S2	7	35
7. ALE inactive delay	2	11
8. MEMW, IOW, MEMR, IOR active delay	4	21
9. MEMW, IOW, MEMR, IOR inactive delay	2	13
10. DEN active delay	3	22
11. DEN inactive delay	6	31
12. DEN active delay	7	31
13. DEN inactive delay	2	18
14. DTR active delay	3	19
15. DTR inactive delay	3	20
16. READY active delay	-3	4

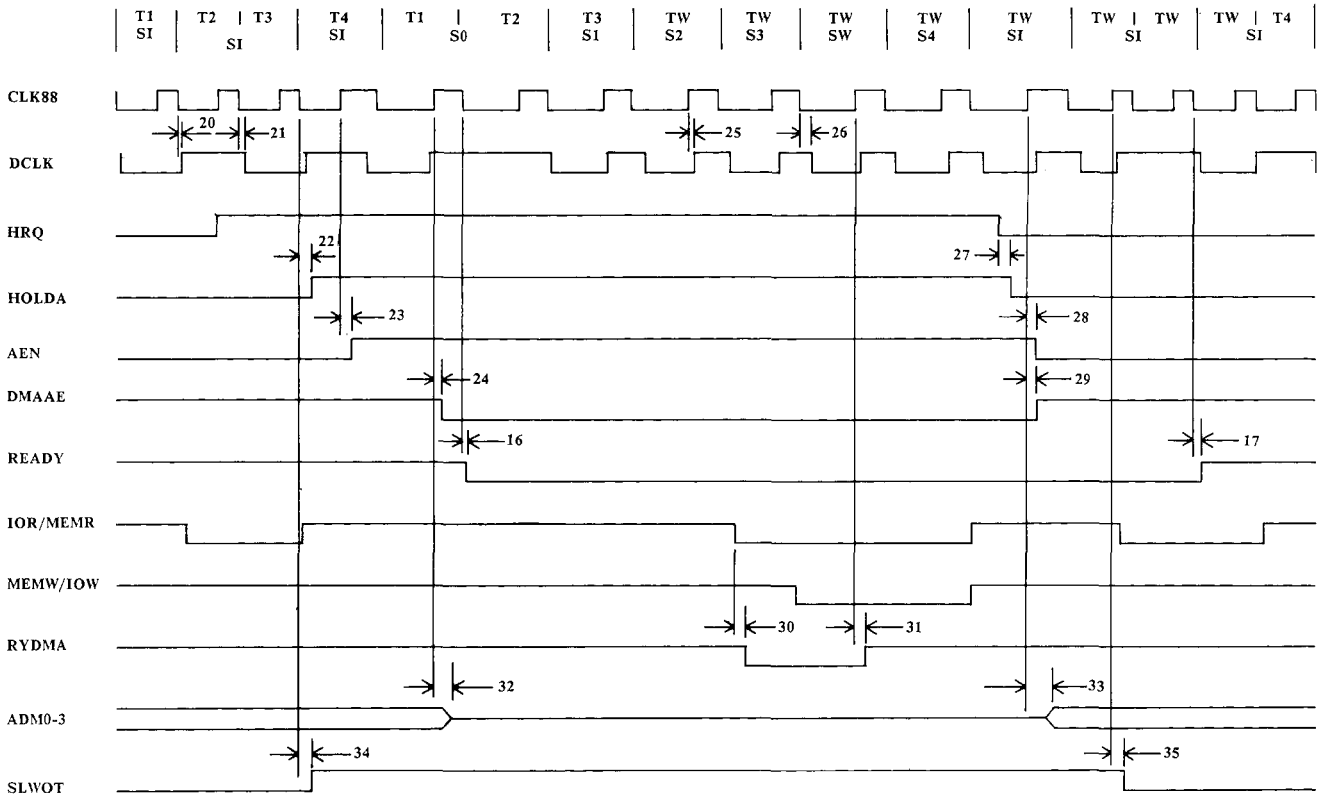
17. READY inactive delay	0	-10
18. EXRES,KYRES setup time	35	
19. SYRES delay	3	18
20. DCLK high delay (CLK88 / 2)	5	25
21. DCLK low delay (CLK88 / 2)	5	27
22. HOLDA delay	4	20
23. AEN active delay	2	10
24. DMAAE active delay	4	24
25. DCLK high delay (CLK88)	3	16
26. DCLK low delay (CLK88)	10	46
27. HOLDA inactive delay	9	45
28. AEN inactive delay	2	18
29. DMAAE inactive delay	2	17
30. RYDMA active delay	12	60
31. RYDMA inactive delay	2	16
32. ADM0-3 tristate delay	7	37
33. AMD0-3 active delay	7	37
34. SLWOT rising delay from CLK88	5	26
35. SLWOT falling delay from CLK88	4	24

36. SLWOT rising delay from IOR, IOW	8	39
37. SLWOT falling delay from IOR,IOW	8	40
38. MWAIT set up time	12	
39. MWAIT hold time	7	
40. IORDY active set up time	58	
41. IORDY inactive set up time	45	
42. DMACS active delay	10	52
43. DMACS inactive delay	7	37
44. NMI active delay from NPNPI	7	38
45. NMI inactive delay from NPNPI	8	44
46. Pulse width of IOCHK	20	
47. NMI active delay from IOCHK	9	47
48. NMI inactive delay from IOW	12	61
49. PARER to PERCK set up time	7	
50. NMI to PERCK delay	8	41
51. SEL58 delay from IOW	9	49
52. DREQ0 delay from DACK0	8	44
53. KBDAT to KBCLK set up time	-420	
54. KBDAT to KBCLK hold time	1260	
55. KDTEN, KCKEN delay from IOW	11	55

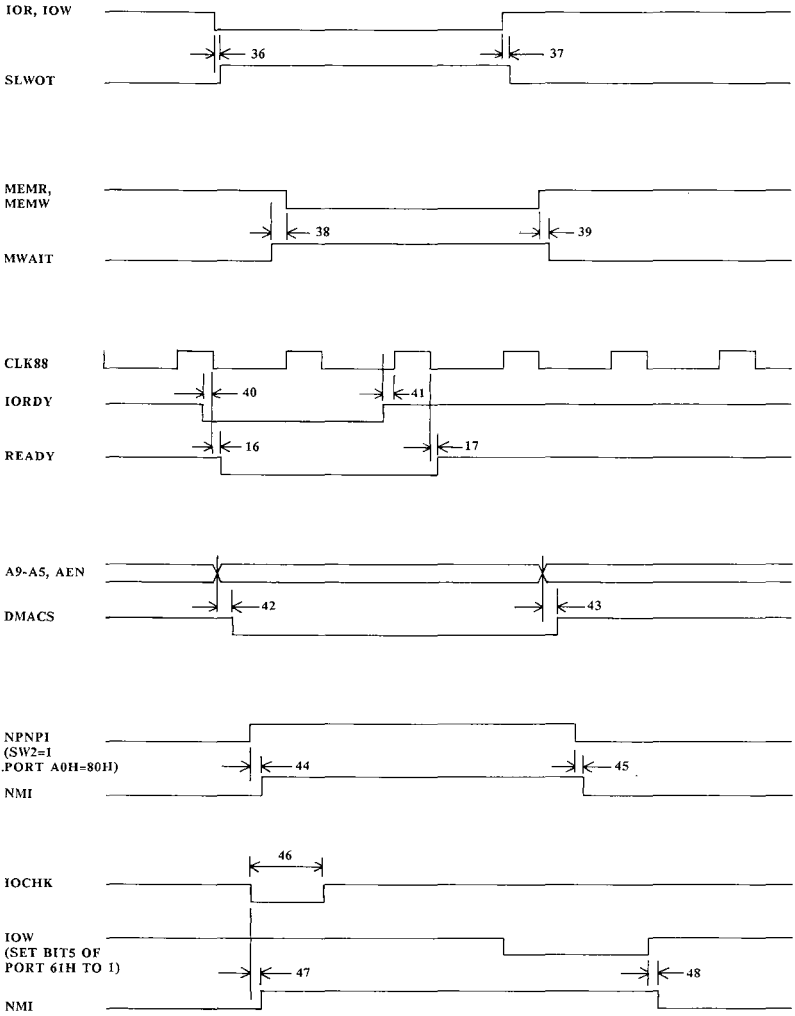
56. DIR active delay from DCNT2, DCNT3	8	39
57. DIR inactive delay from DCNT2, DCNT3	8	39
58. STEP delay from FRSTP, RWSEK	7	37
59. FTRK0 delay from RWSEK, TRK0	7	38
60. RDDAT delay from VC0, SEPDA	7	38
61. PDIR active delay from IOR, IOW	9	46
62. PDIR inactive delay from IOR, IOW	7	37
63. PDIR delay from BUFEN, RTCEN, COMEN, GRDEN	9	45

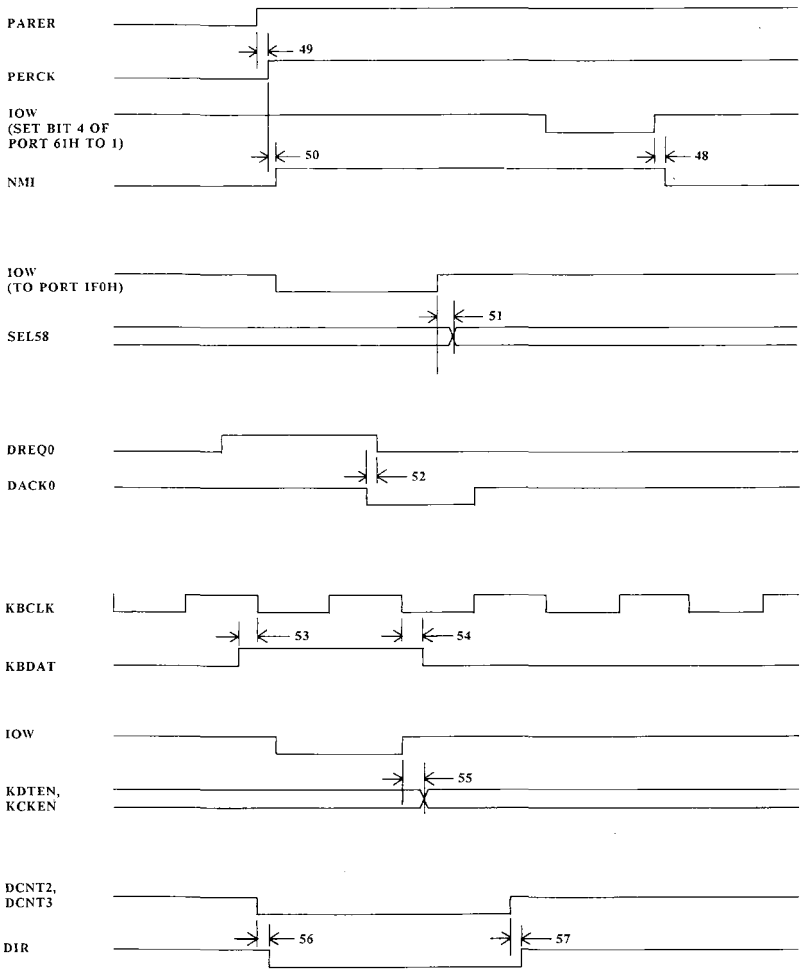


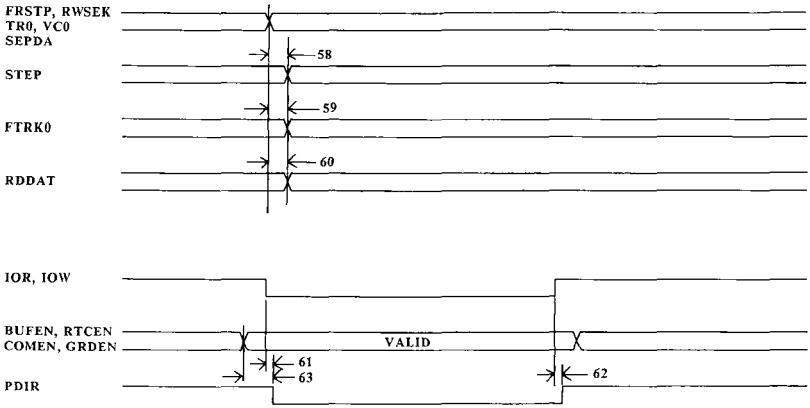
A1 TIMING DIAGRAM



AN EXAMPLE OF DMA TIMING AT HIGH SPEED MODE


IOR, IOW
SLWOT
36
37
MEMR,
MEMW
MWAIT
38
39
CLK88
IORDY
READY
40
41
16
17
A9-A5, AEN
DMACS
42
43
NPNPI
(SW2=1
.PORT A0H=80H)
NMI
44
45
IOCHK
IOW
(SET BIT5 OF
PORT 61H TO 1)
NMI
46
47
48


PARER
49
PERCK
IOW
(SET BIT 4 OF
PORT 61H TO 1)
50
48
NMI
IOW
(TO PORT 1F0H)
51
SEL58
DREQ0
52
DACK0
KBCLK
53
54
KBDAT
IOW
55
KDTEN,
KCKEN
DCNT2,
DCNT3
56
57
DIR


FRSTP, RWSEK
TR0, VC0
SEPDA
STEP
FTRK0
RDDAT
58
59
60
IOR, IOW
BUFEN, RTCEN
COMEN, GRDEN
PDIR
VALID
61
63
62

APPENDIX B

GATE ARRAY
A2 SPECIFICATION

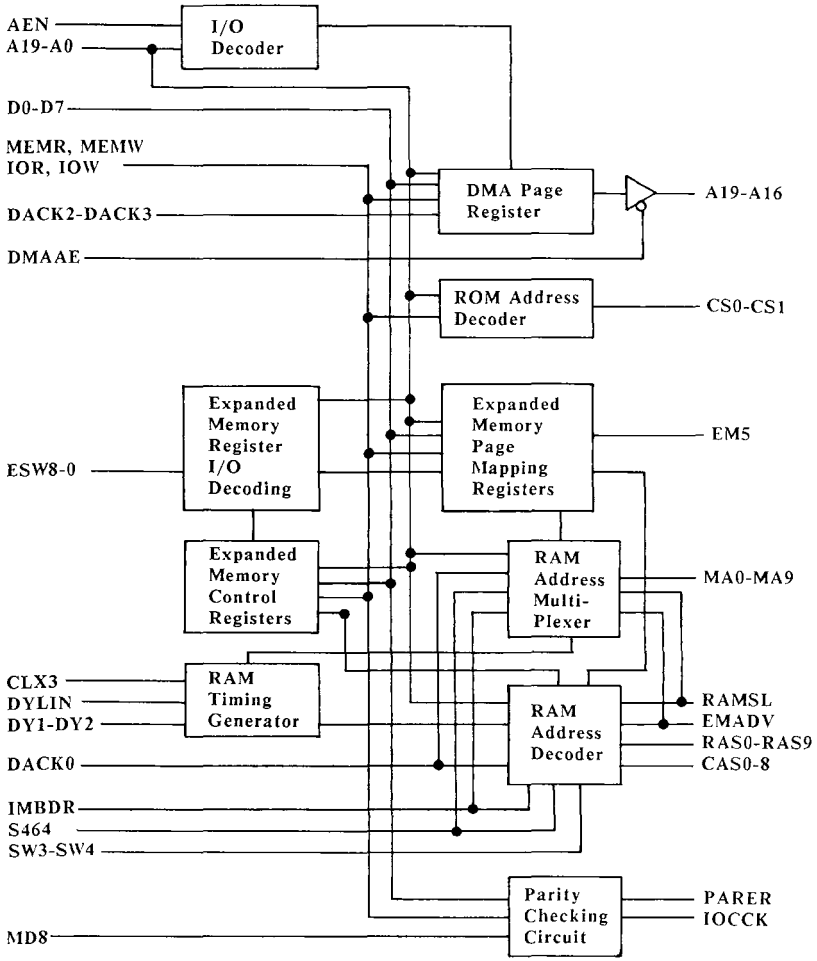
Appendix B
Gate array A2 specification

B.1 A2 functional description

The gate array A2 integrates the following functions:

- Support system RAM up to 640K.
- Support Expanded Memory which conforms to the Lotus® /Intel® Expanded memory standard. A maximum of 4 Mbyte can be added.
- DRAM parity checking circuitry.
- ROM address decoding.
- DMA page register.

B.2 A2 Function diagram



B.3 Gate Array A2 pin usage

Pin No	Pin Type	Name	Description
71	I/O	A19	CPU address line
72	I/O	A18	"
73	I/O	A17	"
74	I/O	A16	" The contents of the DMA page register will be output on A19 - A16 during DMA operation
75	I	A15	CPU address line
76	I	A14	"
77	I	A13	"
78	I	A12	"
79	I	A11	"
80	I	A10	"
81	I	A9	"
82	I	A8	"
83	I	A7	"
84	I	A6	"
85	I	A5	"
86	I	A4	"

87	I	A3	"
88	I	A2	"
89	I	A1	"
90	I	A0	"
62	I/O	D7	CPU data line
61	I/O	D6	"
60	I/O	D5	"
58	I/O	D4	"
56	I/O	D3	"
55	I/O	D2	"
57	I/O	D1	"
59	I/O	D0	"
96	I	IOR	I/O read.
95	I	IOW	I/O write.
94	I	MEMR	Memory read.
93	I	MEMW	Memory write.
42	I	RESET	This is an active low reset signal with schmitt trigger input level.
40	I	DMAAE	DMA address enable Control output of A19 - A16, When it is low, contents of DMA page register will be output on A19-A16.

70	I	AEN	address enable
99	I	DACK0	DMA acknowledge 0
100	I	DACK2	DMA acknowledge 2
98	I	DACK3	DMA acknowledge 3
45	I	SW3	DIP-SW 3
44	I	SW4	DIP-SW 4 SW3 and SW4 are used to select size of system RAM :

SW4	SW3	Size of system RAM
0	0	256 K
0	1	512 K
1	0	576 K
1	1	640 K

52	I	ESW2	ESW2 - ESW0 are used to control
53	I	ESW1	I/O address of Expanded Memory
54	I	ESW0	board 0
49	I	ESW5	ESW5 - ESW3 are used to control
50	I	ESW4	I/O address of Expanded Memory
51	I	ESW3	board 1
46	I	ESW8	ESW8 - ESW6 are used to control
47	I	ESW7	I/O address of Expanded Memory
48	I	ESW6	board 2
97	I/O	MD8	Memory Data Bit 8 It connects directly to bit 8 of DRAM to provide error detection.

34	O	PARER	Parity error output It is the output of the parity checking circuit. It should be connected to the PARER input of gate array A1.
69	OZ	IOCCK	I/O channel check This signal provides parity check for the Expanded Memory. A low indicates parity error. A subsequent memory write will reset it to normal state (tri-stated). System RAM parity error is NOT checked by this signal, so this pin is useful when the A2 is used alone on an Expanded Memory Card.
43	I	CLK88	System Clock input. It should be connected to the CPU clock.
39	I	CKX3	High frequency Clock input. This pin should be tied to a signal which is three times the frequency of CLK88 and synchronized with it. It is used to generated the RAS, CAS and multiplexed address timing.
66	I	DYLIN	Delay line select. When tied to high, all RAM timing will be controlled by an external delay line. For some applications the CKX3 signal is unavailable, then a delay line is necessary for providing RAS and CAS timing.
63	I	DY2	When DYLIN is high, the RAM multiplexed addresses will be controlled by this signal. A low selects column addresses.

64	I	DY1	When DYLIN is high, the CAS signal will be delayed by this signal.
35	O	CS0	ROM 0 Chip Select Memory address range : FE000H - FFFFFH
36	O	Cs1	ROM 1 Chip Select Memory address range : F6000H - FDFFFH
10	O	RAS0	Row address strobe 0
11	O	RAS1	Row address strobe 1
12	O	RAS2	Row address strobe 2
13	O	RAS3	Row address strobe 3
14	O	RAS4	Row address strobe 4
16	O	RAS5	Row address strobe 5
17	O	RAS6	Row address strobe 6
18	O	RAS7	Row address strobe 7
19	O	RAS8	Row address strobe 8
20	O	RAS9	Row address strobe 9
9	O	CAS0	Column address strobe 0
8	O	CAS1	Column address strobe 1
7	O	CAS2	Column address strobe 2
6	O	CAS3	Column address strobe 3
5	O	CAS4	Column address strobe 4

3	O	CAS5	Column address strobe 5
2	O	CAS6	Column address strobe 6
1	O	CAS7	Column address strobe 7
21	O	MA9	Multiplexed address for DRAM
22	O	MA8	"
32	O	MA8A	"
23	O	MA7	"
24	O	MA6	"
25	O	MA5	"
26	O	MA4	"
28	O	MA3	"
29	O	MA2	"
30	O	MA1	"
31	O	MA0	"
37	I	S464	Select 4464 Selects 4464 instead of 41256 as system RAM when this signal is high.
38	I	IMBDR	Select 1 Mbit DRAM When this signal is high, 1 Mbit DRAM can be used to provide 640K of system memory, the remaining 384K is used as Expanded Memory.

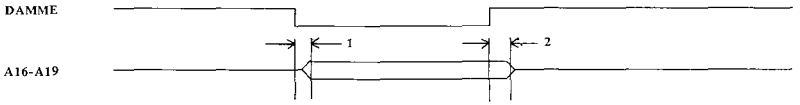
67	O	DIR	Direction control for data transreceiver. For large system, D0-D7 needed be buffered by data transreceiver. A low of DIR indicates data to be read from A2 or the RAM. The data buffer is shared by A2 and the RAM.
68	O	RAMSL	RAM select A low indicates RAM (both system and expanded RAM) is being accessed by the CPU.
92	O	EMADV	Expanded Memory address Valid A low indicates Expanded Memory is being accessed by the CPU.
33	O	EM5	Expanded memory page register Bit 5. When the expanded memory is being accessed by the CPU, bit 5 of the active page register is output on this pin (but inverted). If the expanded memory is implemented using 41256, then this signal can be used with A9 to decode four CAS signals.
4			Not used
27			Not used
15			Ground
65			Ground
41			Vcc
91			Vcc

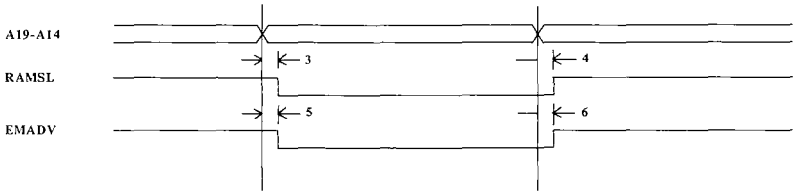
B.4 GATE ARRAY A2 AC CHARACTERISTICS

(Vcc = 5V +/-5%, Ta = 0 TO 70 C, pin capacitive load = 50pF)

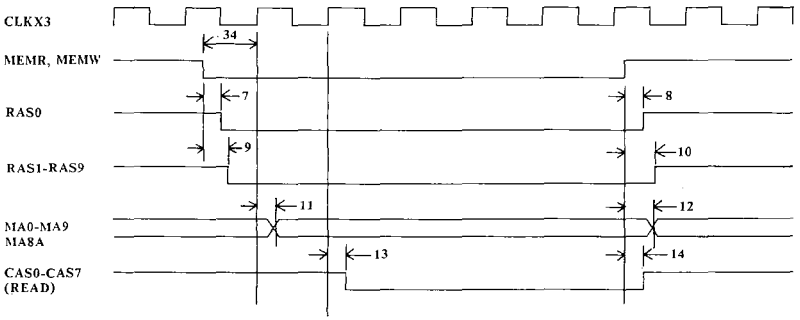
	Min (ns)	Max (ns)
1. A19-A16 active delay	9	41
2. A19-A16 inactive delay	7	33
3. RAMSL active delay	14	63
4. RAMSL inactive delay	14	61
5. EMADV active delay	12	54
6. EMADV inactive delay	11	50
7. RAS0 active delay	8	38
8. RAS0 inactive delay	7	30
9. RAS1-RAS9 active delay	10	45
10. RAS1-RAS9 inactive delay	10	45
11. MA0-MA9 delay from CLKX3	9	44
12. MA0-MA9 delay from MEMR	10	50
13. CAS0-CAS7 delay from CLKX3	12	55
14. CAS0-CAS7 delay from MEMR	9	43
15. CAS0-CAS7 delay from CLK88	10	48
16. MA0-MA9 delay from DY2	10	45
17. MA0-MA9 delay from DY2	10	46

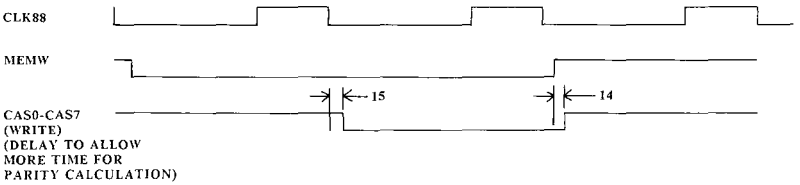
18. CAS0-CAS7 active delay from DY1	12	53
19. CAS0-CAS7 inactive delay from DY1	9	40
20. MD8 tri-state delay	8	39
21. MD8 active delay from MEMR	9	45
22. PARER active delay	10	50
23. PARER inactive delay	10	45
24. IOCHK active delay	9	47
25. MD8 active delay from data	11	51
26. CS0-CS1 active delay MEMR	10	50
27. CS0-CS1 inactive delay from MEMR	8	35
28. DIR active delay from IOR	9	44
29. DIR inactive delay from IOR	8	37
30. D0-D7 active delay	11	55
31. D0-D7 tri-state delay	11	47
32. DIR active delay from MEMR	10	44
33. DIR inactive delay from MEMR	8	36
34. MEMR and MEMW to CLKX3 set up time	15	
35. EM5 delay	20	93



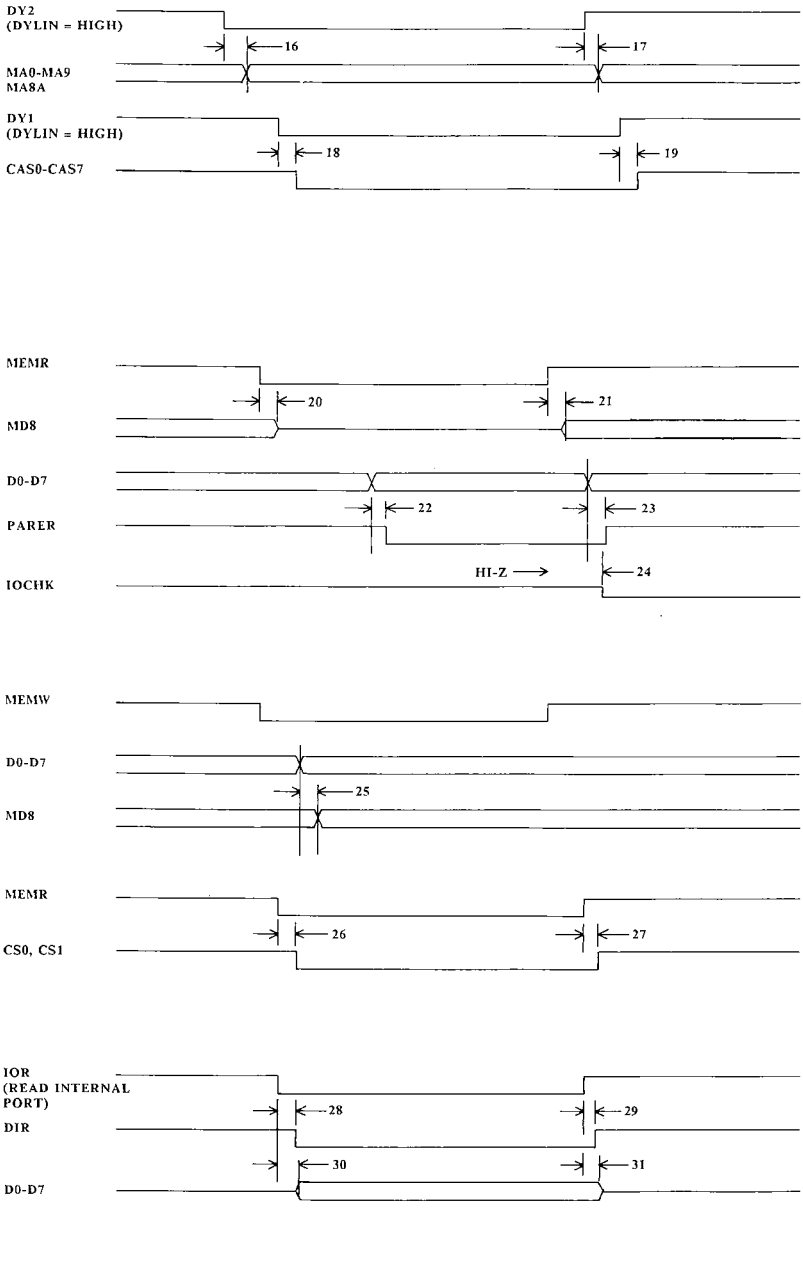


(DYLIN = LOW)

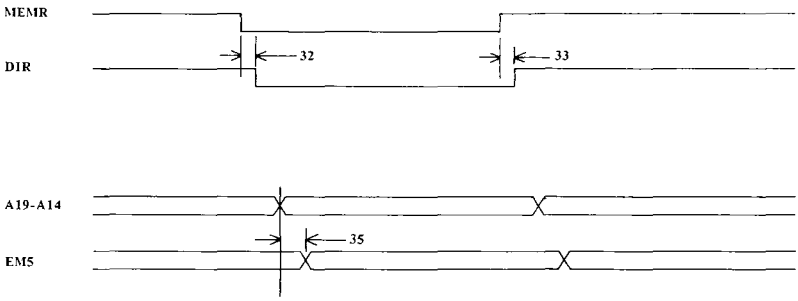




A2 TIMING


DY2
(DYLIN = HIGH)
16
17
MA0-MA9
MA8A
DY1
(DYLIN = HIGH)
18
19
CAS0-CAS7
MEMR
20
21
MD8
D0-D7
22
23
PARER
HI-Z
24
IOCHK
MEMW
D0-D7
25
MD8
MEMR
26
27
CS0, CS1
IOR
(READ INTERNAL
PORT)
28
29
DIR
30
31
D0-D7

A2 TIMING



A2 TIMING

APPENDIX C

8088-1 INSTRUCTION SET

APPENDIX C
8088 INSTRUCTION SET

Mnemonic	Full Name
AAA	ASCII adjust for addition
AAD	ASCII adjust for division
AAM	ASCII adjust for multiplication
AAS	ASCII adjust for subtraction
ADC	Add with carry
ADD	Add
AND	AND
CALL	CALL
CBW	Convert byte to word
CLC	Clear carry flag
CLD	Clear direction flag
CLI	Clear interrupt flag
CMC	Complement carry flag
CMP	Compare
CMPS	Compare byte or word (of string)
CMPSB	Compare byte string
CMPSW	Compare word string
CWD	Convert word to double word
DAA	Decimal adjust for addition
DAS	Decimal adjust for subtraction
DEC	Decrement
DIV	Divide
ESC	Escape
HLT	Halt
IDIV	Integer divide
IMUL	Integer multiply
IN	Input byte or word
INC	Increment
INT	Interrupt
INTO	Interrupt on overflow
IRET	Interrupt return
JA	Jump on above
JAE	Jump on above or equal
JB	Jump on below
JBE	Jump on below or equal

Mnemonic	Full Name
JC	Jump on carry
JCXC	Jump on CX zero
JE	Jump on equal
JG	Jump on greater
JGE	Jump on greater or equal
JL	Jump on less than
JLE	Jump on less than or equal
JMP	Jump
JNA	Jump on not above
JNAE	Jump on not above or equal
JNB	Jump on not below
JNBE	Jump on not below or equal
JNC	Jump on no carry
JNE	Jump on not equal
JNG	Jump on not greater
JNGE	Jump on not greater or equal
JNL	Jump on not less than
JNLE	Jump on not less than or equal
JNO	Jump on not overflow
JNP	Jump on not parity
JNS	Jump on not sign
JNZ	Jump on not zero
JO	Jump on overflow
JP	Jump on parity
JPE	Jump on parity even
JPO	Jump on parity odd
JS	Jump on sign
JZ	Jump on zero
LAHF	Load AH with flags
LDS	Load pointer into DS
LEA	Load effective address
LES	Load pointer into ES
LOCK	LOCK bus
LODS	Load byte or word (of string)
LODSB	Load byte (string)
LODSW	Load word (string)
LOOP	LOOP
LOOPE	LOOP while equal

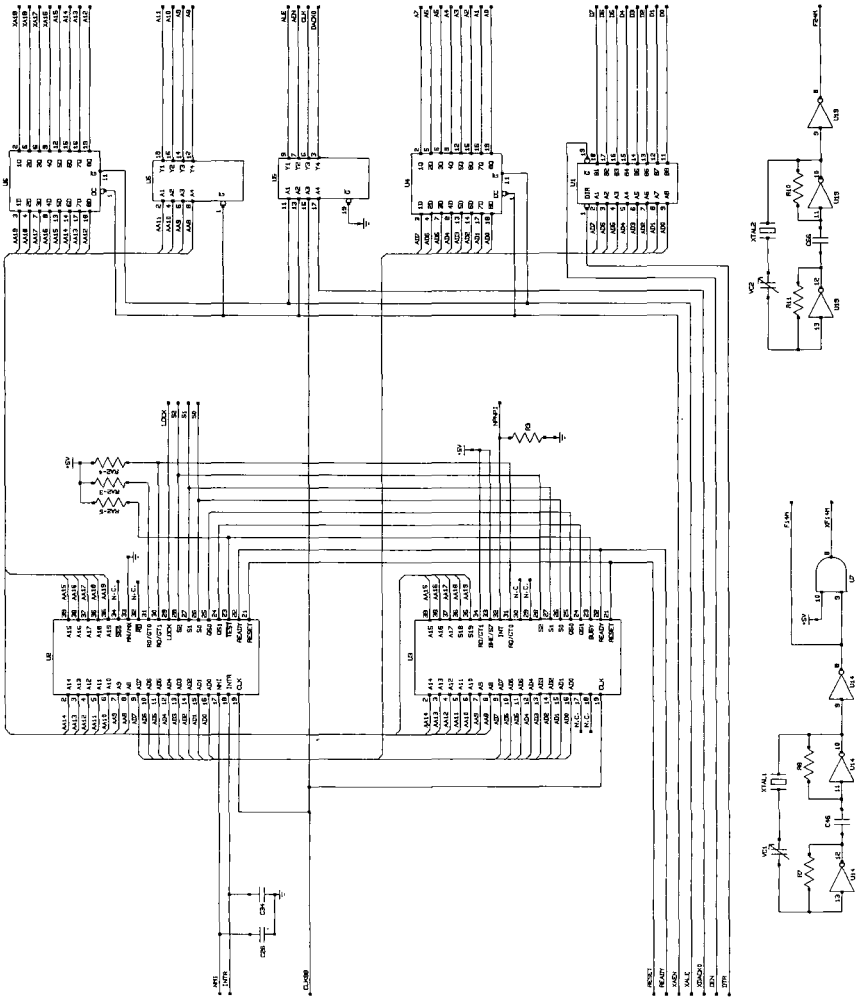
Mnemonic	Full Name
LOOPNE	LOOP while not equal
LOOPNZ	LOOP while not zero
LOOPZ	LOOP while zero
MOV	Move
MOVS	Move byte or word (of string)
MOVSB	Move byte (string)
MOVSW	Move word (string)
MUL	Multiply
NEG	Negate
NOP	No operation
NOT	NOT
OR	OR
OUT	Output byte or word
POP	POP
POPF	POP flags
PUSH	PUSH
PUSHF	PUSH flags
RCL	Rotate through carry left
RCR	Rotate through carry right
REP	Repeat
RET	Return
ROL	Rotate left
ROR	Rotate right
SAHF	Store AH into flags
SAL	Shift arithmetic left
SAR	Shift arithmetic right
SBB	Subtract with borrow
SCAS	Scan byte or word (of string)
SCASB	Scan byte (string)
SCASW	Scan word (string)
SHL	Shift left
SHR	Shift right
STC	Set carry flag
STD	Set direction flag
STI	Set interrupt flag
STOS	Store byte or word (of string)
STOSB	Store byte (string)
STOSW	Store word (string)
SUB	Subtract
TEST	TEST

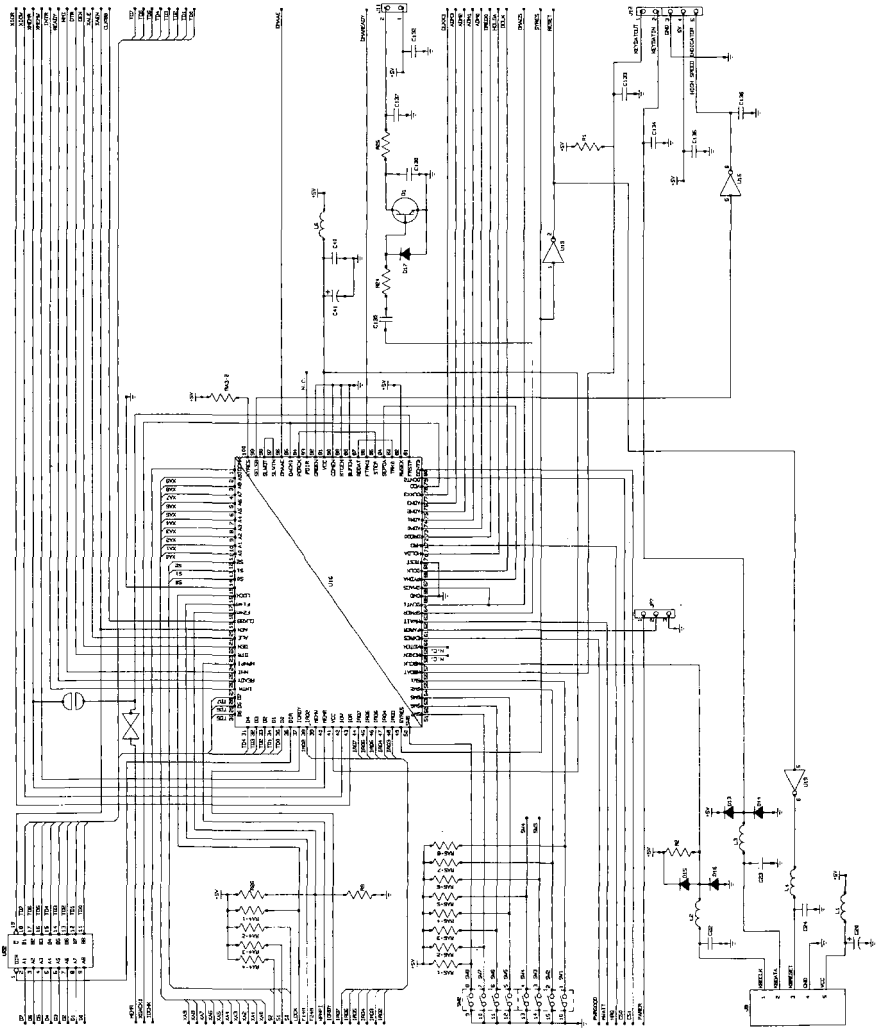
Mnemonic	Full Name
WAIT	WAIT
XCHG	Exchange
XLAT	Translate
XOR	Exclusive OR

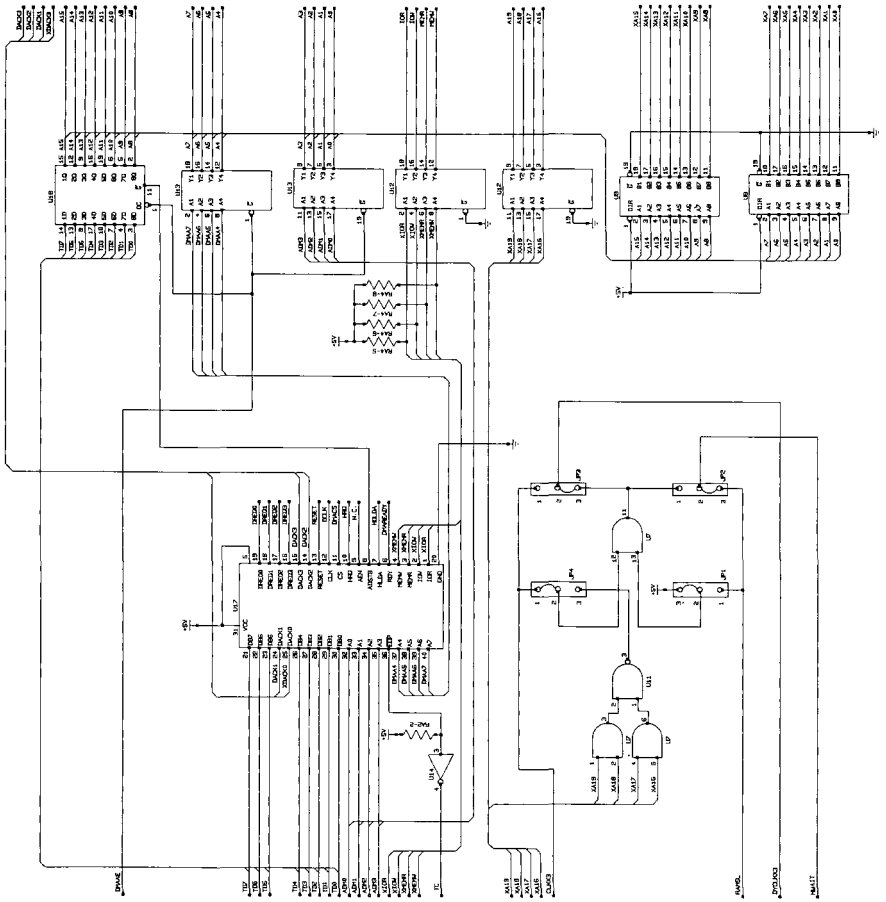
APPENDIX D

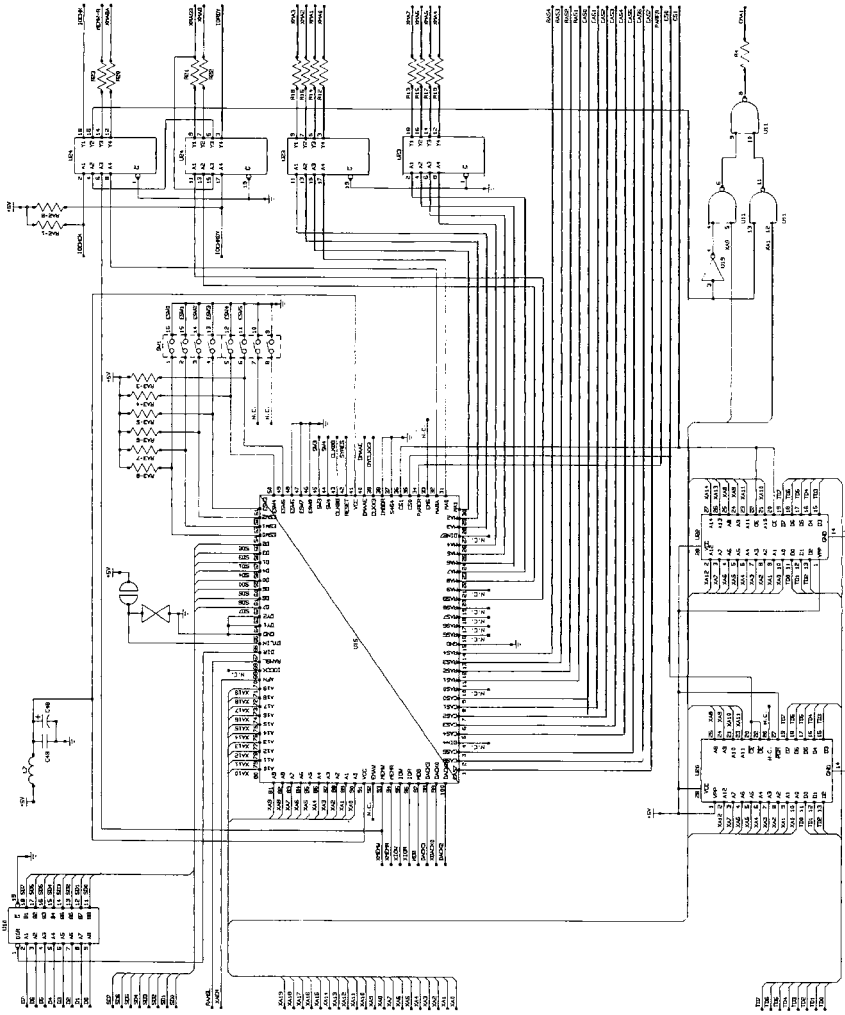
TURBO XT SCHEMATICS

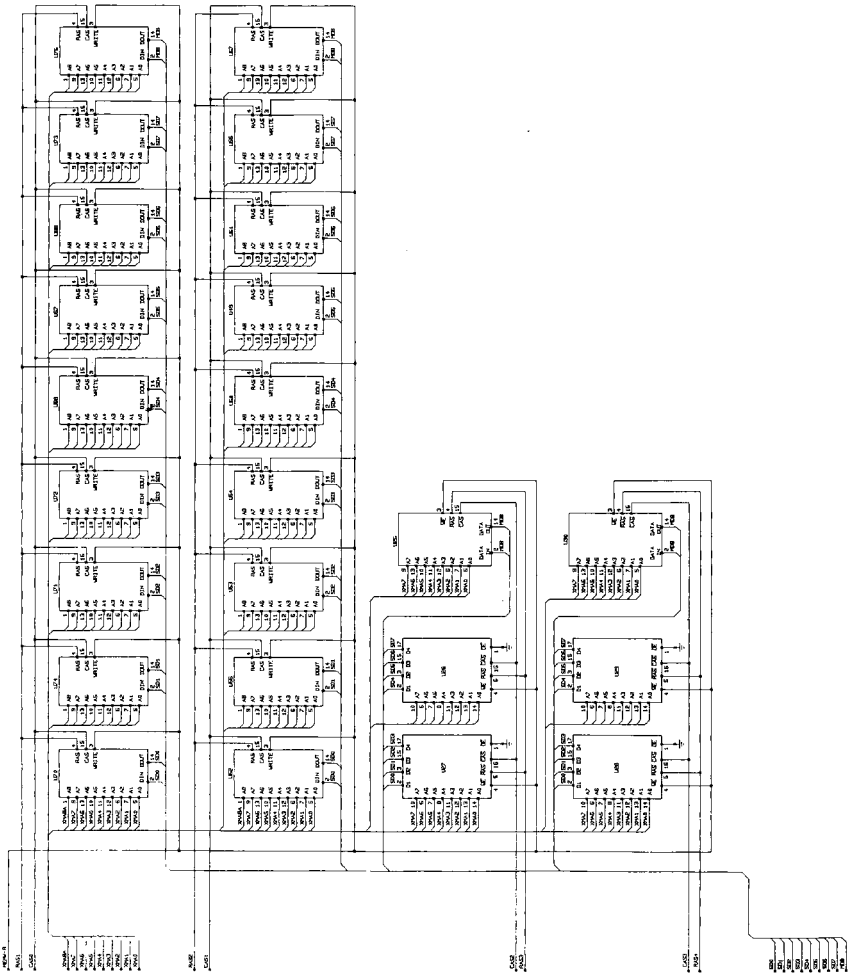
Appendix D
TURBO XT SCHEMATICS

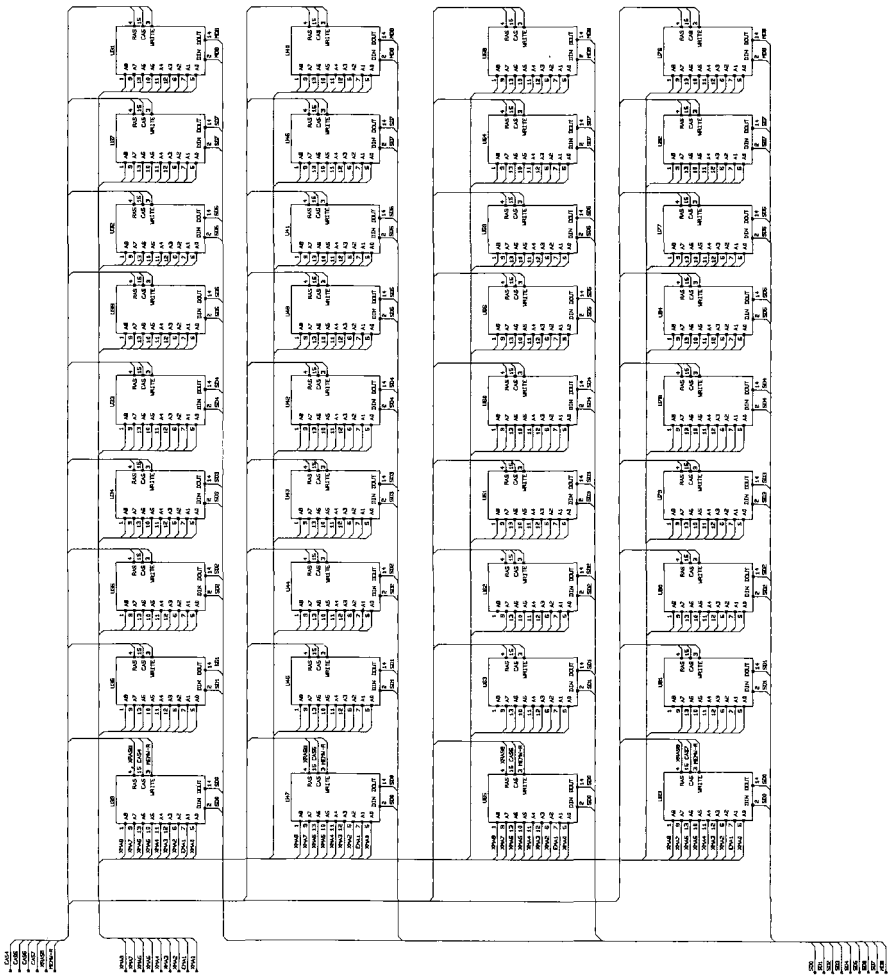


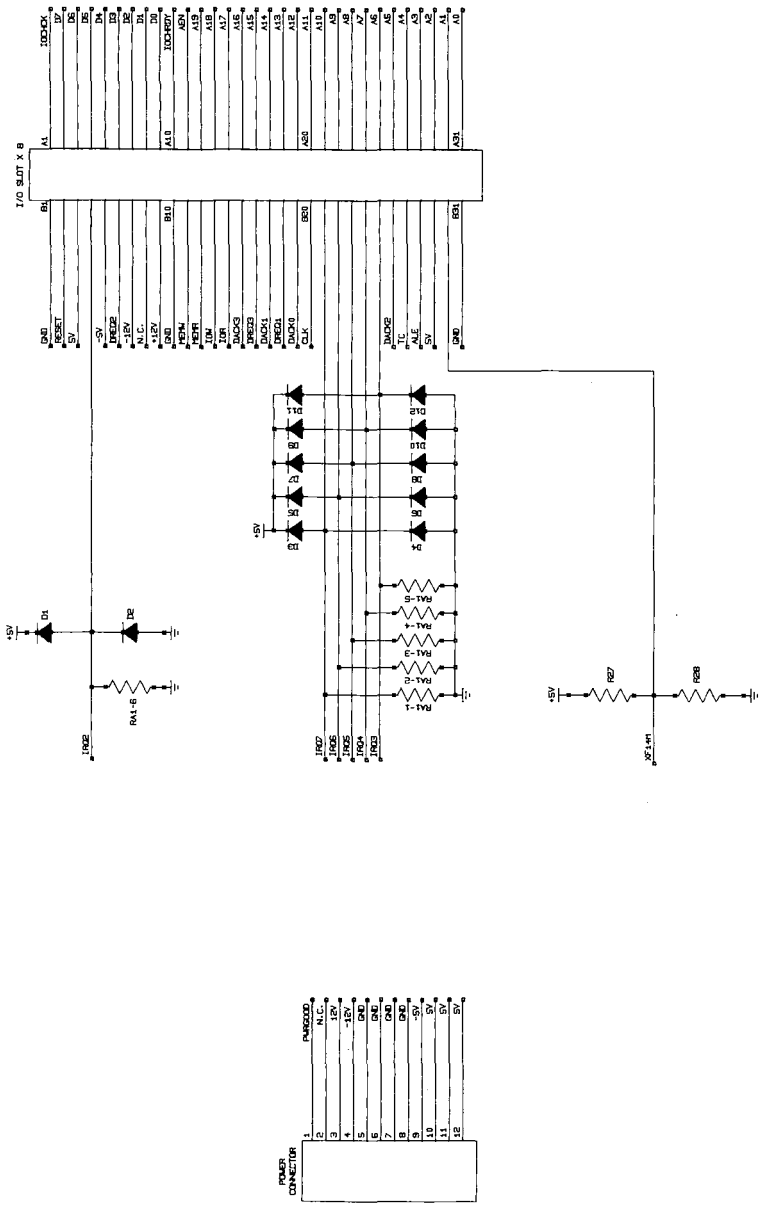











I/O SLOT X 8
POWER CONNECTOR
+5V
IRQ2
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
RA1-1
RA1-2
RA1-3
RA1-4
RA1-5
RA1-6
R27
R28
XF1-H1

APPENDIX E

TURBO XT PART LISTS

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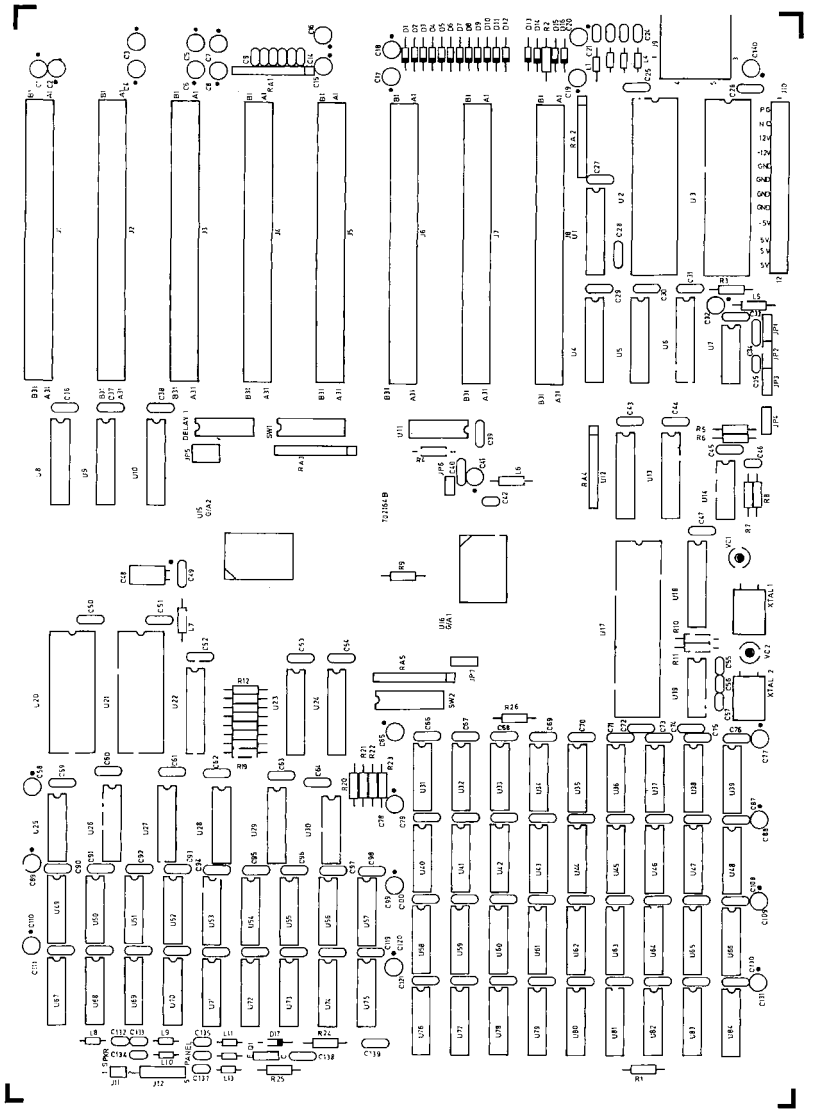

LASER Turbo XT main board component location list

DESTINATION	PART NUMBER	DESCRIPTION
U1,U8-U10,	27-0100-00-01	74LS245 (MOTOROLA)
U22	V27-0100-00-04	74LS245 (TEXAS)
U2	27-0554-01-01	MBL8088-1 (10MHZ) (FUJITSU)
	V27-0554-01-00	P8088-1 (10MHZ) (AMD)
AND	40-0008-00-03	40 PINS I.C. SOCKET (DOUBLE CONTACT)
	40-0008-00-00	40 PINS I.C. SOCKET (DOUBLE CONTACT)
U3	40-0008-00-03	40 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0008-00-00	40 PINS I.C. SOCKET (DOUBLE CONTACT)
U4,U6,U18	27-0183-00-00	74LS373 (HITACHI)
	V27-0183-00-01	74LS373 (MOTOROLA)
	V27-0183-00-02	74LS373N (TEXAS)
U5,U12,U13	27-0160-00-00	74LS244 (MOTOROLA)
U7	27-0184-00-00	74LS08 (HITACHI)
	V27-0184-00-04	74LS08 (TEXAS)
	V27-0184-00-05	74LS08 (MOTOROLA)
U11	27-0037-01-00	HD74LS00N (HITACHI)
	V27-0037-01-03	74LS00 (MOTOROLA)
	V27-0037-01-06	74LS00 (MOTOROLA)
	V27-0037-01-07	74LS00N (TEXAS)
U14	27-0038-02-00	HD74LS04 (HITACHI)
	V27-0038-02-03	74LS04 (MOTOROLA)
	V27-0038-02-05	74LS04N
	V27-0038-02-06	74LS04 (SGS)
U15	27-0603-00-00	GATE ARRAY A2
U16	27-0602-01-00	GATE ARRAY A1.1
	R27-0602-00-00	GATE ARRAY A1
U17	27-0488-00-00	8237A-5 DMA CONTROLLER (NEC)
	V27-0488-00-01	P8237A-5 DMA CONTROLLER (AMD)
	V27-0488-00-02	P8237A-5 DMA CONTROLLER (INTEL)
U19	27-0038-03-00	74S04 (TEXAS)
	V27-0038-03-03	HD74S04 (HITACHI)
U20	27-0672-00-03	MASK ROM R09864D-196 (200NS)
	A27-0143-03-00	EPROM 2764-20 (200NS) (HITACHI)
	A27-0143-02-04	EPROM TMS2764-25 (250NS) (TEXAS)
AND	40-0007-00-04	28 PINS I.C. SOCKET

		(DOUBLE CONTACT)
	V40-0007-00-00	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-02	28 PINS I.C. SOCKET (DOUBLE CONTACT)
U21	40-0007-00-04	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-00	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-02	28 PINS I.C. SOCKET (DOUBLE CONTACT)
U23,U24	27-0451-00-00	74S244 (TEXAS)
U26-U29	40-0067-00-03	18 PINS I.C. SOCKET (DOUBLE CONTACT)
	A40-0067-01-00	18 PINS I.C. SOCKET (DOUBLE CONTACT)
U25,U30, U31-U39,	40-0082-01-01	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U40-U48, U49-U57,	A40-0625-16-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U58-U66, U76-U84	V40-0082-01-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U67-U75	27-0532-03-00	DRAM HM50256P-12 (256K X 1) (HITACHI)
	V27-0532-03-01	DRAM MT1259-12 (256K X 1) (MICRON)
	V27-0532-03-02	DRAM MCM6256AP12 (256K X 1) (MOTOROLA)
	V27-0532-03-03	DRAM TMM41256P-12 (256K X 1) (TOSHIBA)
	V27-0532-03-04	DRAM KM41256-12 (256K X 1) (SAMSUNG)
AND	40-0082-01-01	16 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0082-01-00	16 PINS I.C. SOCKET (DOUBEL CONTACT)
	A40-0082-01-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
R1,R2	23-0472-10-02	RESISTOR 4.7K OHM 1/4W +/-5%
	V23-0472-10-00	RESISTOR 4.7K OHM 1/4W +/-5%
R3	23-0015-10-02	RESISTOR 100K OHM 1/4W +/-5%
	V23-0015-10-00	RESISTOR 100K OHM 1/4W +/-5%
R4,R12-R23	23-0270-10-02	RESISTOR 27K OHM 1/4W +/-5%
R5,R6	(NOT USED)	
R7,R8	23-0013-10-02	RESISTOR 1K OHM 1/4W +/-5%
	V23-0013-10-00	RESISTOR 1K OHM 1/4W +/-5%

R9,R26	23-0561-10-02	RESISTOR 560 OHM 1/4W +/-5%
R10,R11	23-0221-10-02	RESISTOR 220 OHM 1/4W +/-5%
	V23-0221-10-00	RESISTOR 220 OHM 1/4W +/-5%
R24	23-0222-10-02	RESISTOR 2.2K OHM 1/4W +/-5%
	V23-0222-10-00	RESISTOR 2.2K OHM 1/4W +/-5%
R25	23-0470-10-02	RESISTOR 47 OHM 1/4W +/-5%
	23-0470-10-00	RESISTOR 47 OHM 1/4W +/-5%
RA1	26-1103-08-01	RESISTOR NETWORK 10K OHM X 8,9 PINS
	V26-1103-08-05	RESISTOR NETWORK 10K OHM X 8,9 PINS
RA2,RA3,RA5	26-1472-08-13	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-00	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-01	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-02	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-05	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
RA4	26-1332-08-06	RESISTOR NETWORK 3.3K OHM X 8,9 PINS
	V26-1332-08-00	RESISTOR NETWORK 3.3K OHM X 8,9 PINS
XTAL 1	25-3015-00-00	CRYSTAL 14.31818 MHZ +/-30PPM
	V25-3015-00-04	CRYSTAL 14.31818 MHZ +/-30PPM
XTAL 2	25-3063-00-01	CRYSTAL 30 MHZ +/-30PPM
	V25-3063-00-00	CRYSTAL 30 MHZ +/-30PPM
Q1	20-0028-02-00	TRANSISTOR NA31XJ
	A20-0028-04-00	TRANSISTOR NA31X I/J/H
L1-L4	25-1109-00-00	3 1/2T FERRITE BEAD CHOKE HOR.
	V25-1109-00-01	3 1/2T FERRITE BEAD CHOKE HOR.
L5-L7	25-1020-00-00	CHOKE COIL 3.3UH
	V25-1020-00-02	CHOKE COIL 3.3UH
L8-L13	(SHORTED IN PCB)	
D1-D17	21-0001-00-00	DIODE IN4148
SW1,SW2	42-0055-00-00	DIP SWITCH 8 POLES (SLIDE TYPE)
	V42-0055-00-04	DIP SWITCH 8 POLES (SLIDE TYPE)

	V42-0055-00-06	DIP SWITCH 8 POLES (SLIDE TYPE)
VC1,VC2	22-7002-01-00	TRIMMER CAP 4PF-20PF +80-0%
	A22-7002-00-00	TRIMMER CAP 20FP
	V22-7002-00-12	TRIMMER CAP 20PF
C2-C5,	22-1470-21-03	ELEC CAP 47UF 16V +/-20%
C65,C99,	V22-1470-21-11	ELEC CAP 47UF 16V +/-20%
C120	V22-1470-21-16	ELEC CAP 47UF 16V +/-20%
	V22-1470-21-51	ELEC CAP 47UF 16V +/-20%
C19-C20	22-1100-21-00	ELEC CAP 10UF 16V +/-20%
	V22-1100-21-03	ELEC CAP 10UF 16V +/-20%
C21-C24	22-3102-28-00	CER CAP 0.001UF 50V +80/-20%
	A22-3102-26-00	CER CAP 1000PF 50V +/-10%
	A22-3102-28-15	CER CAP 1000PF 50V +80/-20%
C25-C27,C33	22-3104-28-33	MONO CAP 0.1UF 50V +80/-20%
C29-C31,	V22-3104-28-40	MONO CAP 0.1UF 50V +80/-20%
C36-C40,	V22-3104-28-53	MONO CAP 0.1UF 50V +80/-20%
C43-C45,C47, C49-C54, C59-C64, C66-C76, C79-C87, C90-C98, C100-C108, C111-C119,C121, C123-C130, C138-C139		
C122	(NOT IN USE)	
C28	22-3471-26-00	CER CAP 470PF 50V +/-10%
C32,C41,C48	22-1109-61-03	ELEC CAP 1UF 50V +/-20%
	V22-1109-61-04	ELEC CAP 1UF 50V +/-20%
C34	22-3331-26-00	CER CAP 330PF 50V +/-10%

C46	22-3470-26-00	CER CAP 47PF 50V +/-10%
	A22-3470-25-00	CER CAP 47PF 50V +/-5%
	A22-3470-26-01	CER CAP 47PF 50V +/-10%
C56	22-3101-26-00	CER CAP 100PF 50V +/-10%
C58,C77,C88	22-1101-11-03	ELEC CAP 100UF 10V +/-10%
C89,C109, C110,C131		
C1,C6-C8, C9-C14, C15-C18,C35, C42,C55,C57, C78,C132-C137	(NOT USED)	
J1-J8	40-0472-00-00	PCB EDGE CONNECTOR 62 WAYS
J9	40-0459-05-00	DIN SOCKET (WITH SHIELDS) 5 PINS
J10	40-0500-12-00	HEADER (POWER)
J11	40-0118-00-01	CONNECTOR WAFER 2 PINS (RIGHT ANGLE)
	V40-0118-00-00	CONNECTOR WAFER 2 PINS (RIGHT ANGLE)
J12	40-0120-00-01	CONNECTOR WAFER 5 PINS (RIGHT ANGLE)
	V40-0120-00-00	CONNECTOR WAFER 5 PINS (RIGHT ANGLE)
JP1-JP5	(SHORTED IN PCB)	
JP6	(NOT USED)	
JP7	40-0215-00-01	WAFER 3 PINS
	V40-0215-00-00	WAFER 3 PINS
AND	40-0342-00-00	2-CONTACT SHORT CIRCUIT SOCKET
	A40-0342-01-00	SHUNT CONNECTOR
	A40-0342-02-00	SHUNT CONNECTOR

91-2096-11