SYSTEM BOARD

Pentium™ M.B.

OPTI 596/597

EXP5084

SERIES

CONTENTS

CHAPTER 1 INTRODUCTION

The OPTI PTMA WB-V chipset provides a highly integrated solution for fully compatible, high performance PC/AT platforms. Together with the 82C206 integrated peripherals controller, this chipset will support the Pentium™ [1] microprocessor in the most cost effective and feature-rich designs available today. Since the chipset is so critical to the performance and cost structure of a PC,this highly integrated approach provides the foundation for a cost effective platform without compromising performance. The OPTI PTMA WB-V chipset provides a powerful solution positioned to deliver value without neglecting quality, compatibility or reliability.

The PTMA WB-V chipset is comprised of two chips, the 82C597 SYSC controller and 82C596 ATC controllor.The SYSC provides the control functions for the host CPU interface,the 32-bit Local bus interface,the 64-bit Level 2 (L2) cache and the 64-bit DRAM bus.The SYSC also controls the data flow between the CPU bus,the DRAM bus,the Local bus and the 16/8-bit ISA bus.A complete Pentium solution consists of the PTMA WB-V chipset and an 82C206 integrated peripherals controller (IPC).

The 82C596 ATC integrates the AT bus interface and the data buffers for transfers between the CPU data bus,Local data bus and the DRAM data bus.It also provides ISA to Local bus command translation.

SYSTEM FEATURES

- Fully supports the Pentium microprocessor.
- Supports Pentium CPU address pipelining.
- 1X clock source,supporting systems running up to 66 MHz.
- Write Back,cirect-mapped cache with size selections : 64K,128K,256K,512K.
- Programmable cache write policy : Write Back or Write Through.
- Fully programmable cache and DRAM read/write cycles.
- Supports 3-2-2-2 cache burst read cycle at 66 MHz.
- Supports two banks of 64-bit wide DRAMs with256K,512K,1M,2M,4M and 8M x 36 page-mode DRAMs.
- Supports DRAM configurations up to 128MB.
- Supports 3-3-3-3 pipeline DRAM burst cycles.
- Shadow RAM option.
- Hidden refresh with CAS before RAS refresh supported.
- High performance 32-bit Local Bus support.
- Performance-oriented snoop-line comparator for VL/ISA bus masters.
- Extended DMA page register.
- Asynchronous CPU and VL bus interface.
- AT Bus Clock speed programmability.

SYSTEM PERFORMANCE

LANDMARK SPEED (VER : 0.99)	587.2MHz
LANDMARK SPEED (VER : 1.14)	200+MHz
LANDMARK SPEED (VER : 2.0)	346.5MHz
POWER METER **MIPS** (VER : 1.7)	41.5MIPS
NORTON **CPU SPEED** (VER 6.0)	190.3

SYSTEM SPECIFICATION

Processor :	Pentium
CPU Clock :	60 / 66 MHz Pentium M/B
CPU Clock Source :	OSCILLATOR
Memory :	up to 128MB
Memory configuration :	2M/4M/6M/8M/10M/12M/16M/18M/20M/24M/ 32M/34M/36M/40M/48M/64M/66M/68M/72M/ 80M/96M/128M
Memory using :	256K/512K/1M/2M/4M/8M 36bit Module,memory up to 128MB on board
SRAM configuration :	64KB/128KB/256KB/512KB
BIOS Subsystem :	AMI ROM BIOS

Additional BIOS features : Set program resides in ROM.

I/O Subsystem NO. slot : SIX 16 bit & ONE 8 bit ISA Slots,TWO 32 bit Local Bus.

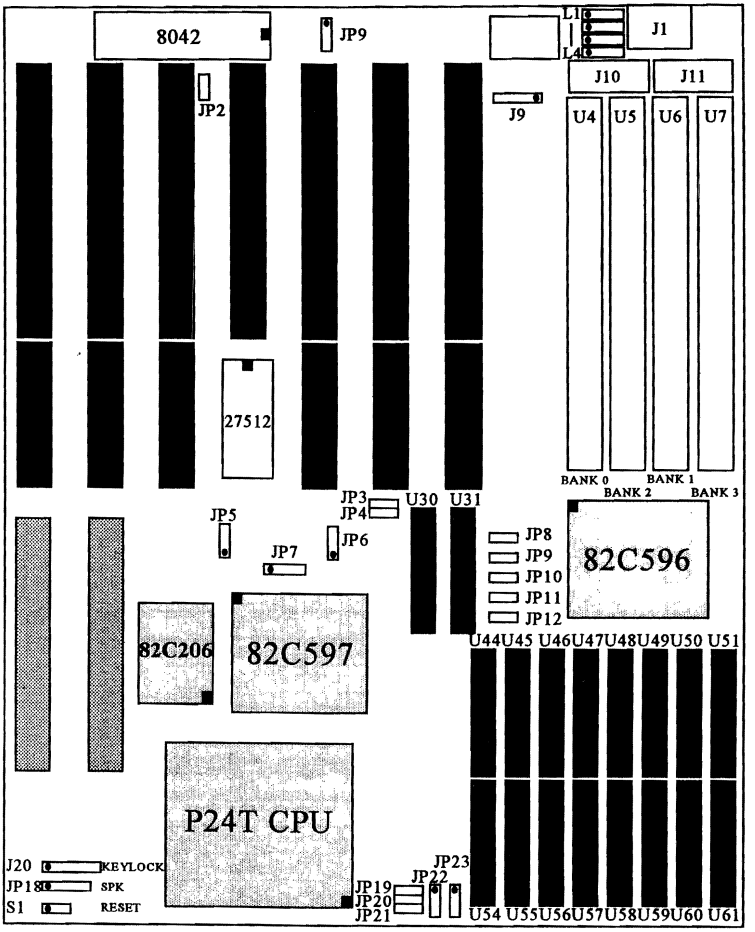
Dimension : 12" x 8.6" , Baby AT size.

Additional features

Miscellanous connectors : Reset buttem. Internal battery.

Board design : SIX layer implementation for low noise operation.

OPTI-PENTIUM MOTHERBOARD LAYOUT



CHAPTER 2 INSTALLATION

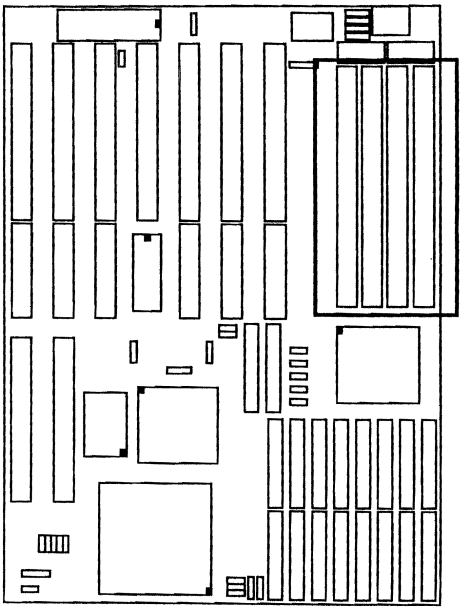
BEFORE TURNING ON THE SYSTEM POWER , PLEASE FOLLOW THE FOLLOWING INSTRUCTIONS CAREFULLY OR YOUR SYSTEM MAY NOT OPERATE CORRECTLY. THANK YOU ! !

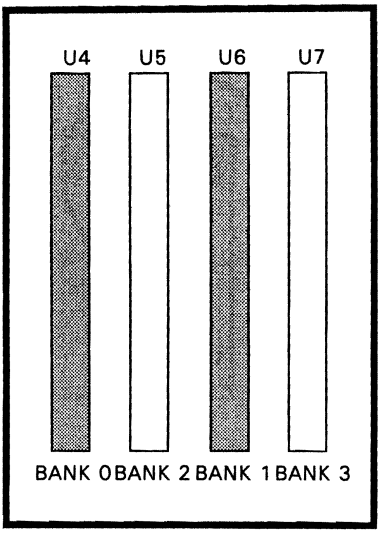
ON BOARD SIMM INSTALLATION

The OPTI-Pentium motherboard memory can expanded memory from 2M to 128M. Either 256K, 512K ,1M ,2M ,4M ,8M SIM DRAM can be used the OPTI-Pentium motherboard.There are spacial BANK 0,BANK 1,BANK 2,BANK 3 SIMM of assembly available for the OPTI-Pentium motherboard.

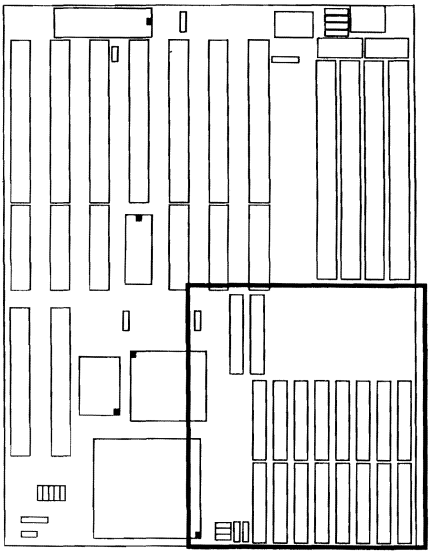
BANK 0	BANK 1	BANK 2	BANK 3	TOTAL
256K	256K	NONE	NONE	2M
512K	512K	NONE	NONE	4M
1M	1M	NONE	NONE	8M
2M	2M	NONE	NONE	16M
4M	4M	NONE	NONE	32M
8M	8M	NONE	NONE	64M
256K	256K	256K	256K	4M
256K	256K	512K	512K	6M
512K	512K	512K	512K	8M
256K	256K	1M	1M	10M
512K	512K	1M	1M	12M
1M	1M	1M	1M	16M
256K	256K	2M	2M	18M
512K	512K	2M	2M	20M
1M	1M	2M	2M	24M
2M	2M	2M	2M	32M
256K	256K	4M	4M	34M
512K	512K	4M	4M	36M
1M	1M	4M	4M	40M
2M	2M	4M	4M	48M
4M	4M	4M	4M	64M
256K	256K	8M	8M	66M
512K	512K	8M	8M	68M
1M	1M	8M	8M	72M
2M	2M	8M	8M	80M
4M	4M	8M	8M	96M
8M	8M	8M	8M	128M

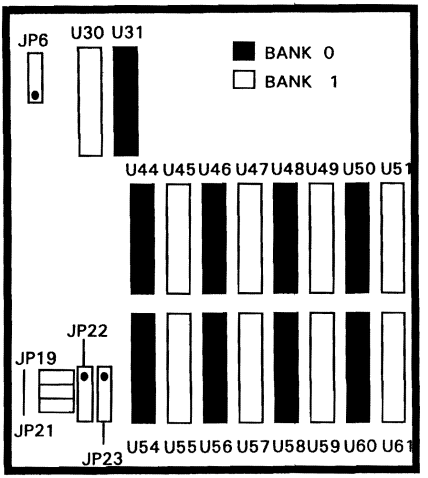
SIMM MODULE DRAM on the motherboard consisfirst of BANK 0 - 3. When you install the DRAM on the motherboard,first completely fill BANK 0 and BANK 1,then fill BANK 2 and BANK 3.The spaces of BANK 0 and BANK 1 should be fully occupied,otherwise the motherboard will not work.

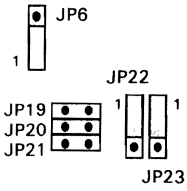
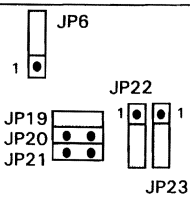
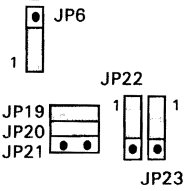
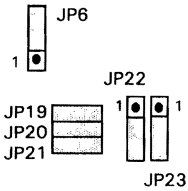




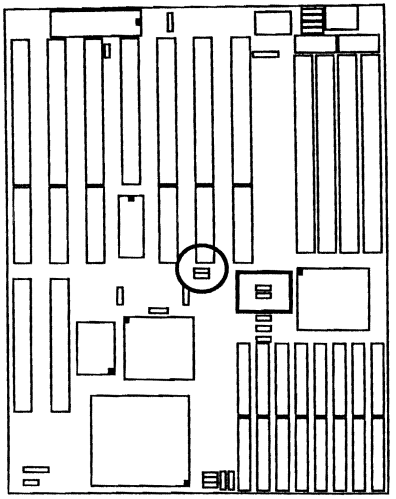
CACHE SRAM INSTALL SELECTION

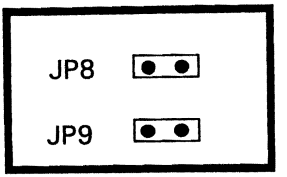


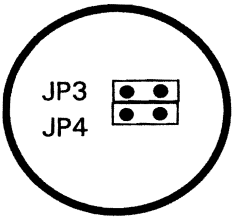


CACHE RAM SIZE			
64K	128K	256K	512K
TAG RAM : U31 (8KX8) DATA RAM : BANK 0 (8KX8)	TAG RAM : U31 (8KX8) DATA RAM : BANK 0 (8KX8) BANK 1 (8KX8)	TAG RAM : U31 (8KX8) DATA RAM : BANK 0 (32KX8)	TAG RAM : U30,U31 (8KX8) DATA RAM : BANK 0 (32KX8) BANK 1 (32KX8)
			

JUMPER SETTING





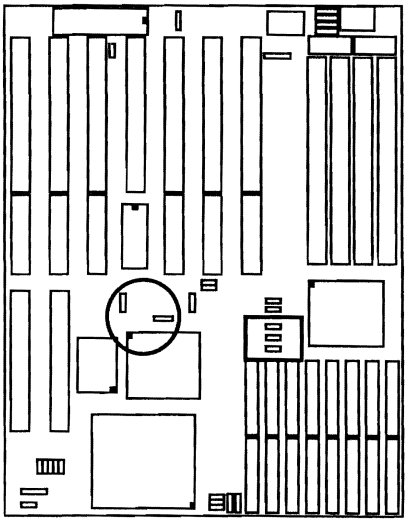


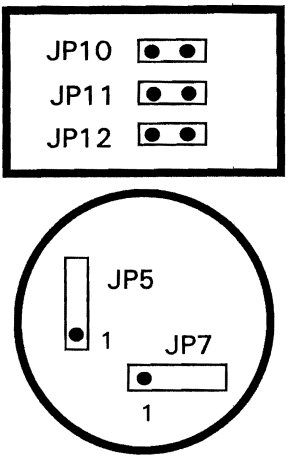
ATCLK SELECTION

LCLK / 5	LCLK / 4	LCLK / 3	LCLK / 2
JP 8	JP 8	JP 8	JP 8
JP 9	JP 9	JP 9	JP 9

JP3	MDHDOE# INACTIVE
	END OF LAST T2
	BEGINNING OF LAST T2

JP4	LCLK SOURCE
	EXTERNAL SOURCE
	INTERNAL / SYNCRONOUS (LCLK = LCLK/2)





JP5	USAGE
1	EXTERNAL LCLK
1	INTERNAL LCLK

JP7	USAGE
1	LCLK WITH 74F08 BUFFER
1	INTERNAL LCLK DIRECTLY DRIVE VESA

JP10	BACK TO BACK IO DELAY
	ENABLED
	DISABLED

JP11	LEDV* SAMPLE SELECTION
	END OF SECOND T2
	END OF FIRST T2

JP12	LOCAL BUS DISABLE
	VL-BUS DISABLED
	VL-BUS ENABLED

FUNCTION CONNECTOR

J1 : KEYBOARD CONNECTOR

PIN	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	SPACE
4	GROUND
5	+ 5V DC

JP18 : SPEAKER CONNECTOR

PIN	DESCRIPTION
1	DATA OUT
2	NOT USED
3	GROUND
4	+ 5V

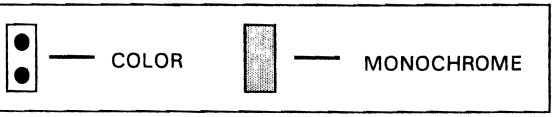
S1 : RESET SW CONNECTOR

PIN	DESCRIPTION
1	GROUND
2	RESET IN

J20 : KEYLOCK CONNECTOR

PIN	DESCRIPTION
1	LED POWER
2	NOT USED
3	GROUND
4	KEYBOARD INHIBITER
5	GROUND

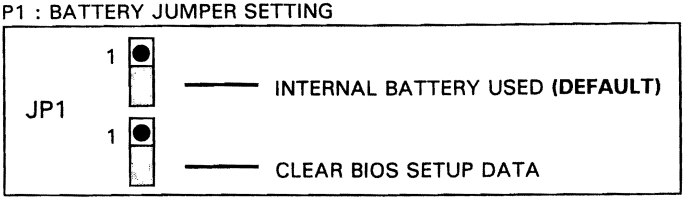
JP2 : DISPLAY ADAPTER SET UP



J9 : EXTERNAL BATTERY CONNECTOR

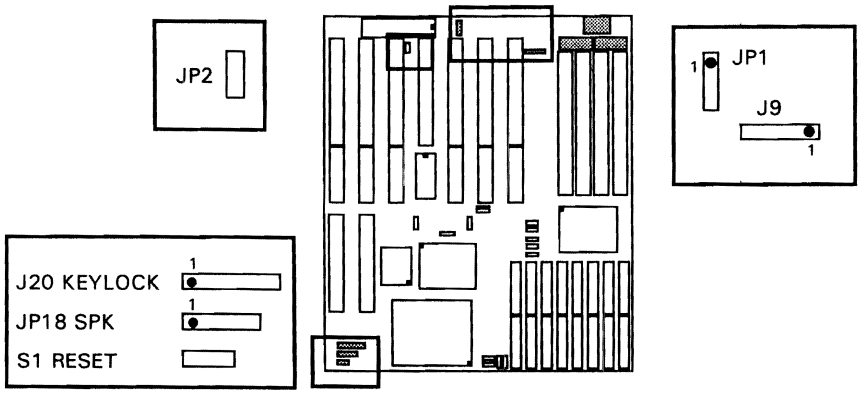
PIN	DESCRIPTION
1	BATTERY (+)
2,3	N.C.
4	GROUND

JP1 : BATTERY JUMPER SETTING



J10,J11 : POWER SUPPLY CONNECTOR

CONNECTOR	PIN	DESCRIPTION
J10	1	POWER GOOD
	2	+ 5V DC
	3	+ 12V DC
	4	- 12V DC
	5	GROUND
	6	GROUND
J11	1	GROUND
	2	GROUND
	3	- 5V DC
	4	+ 5V DC
	5	+ 5V DC
	6	+ 5V DC



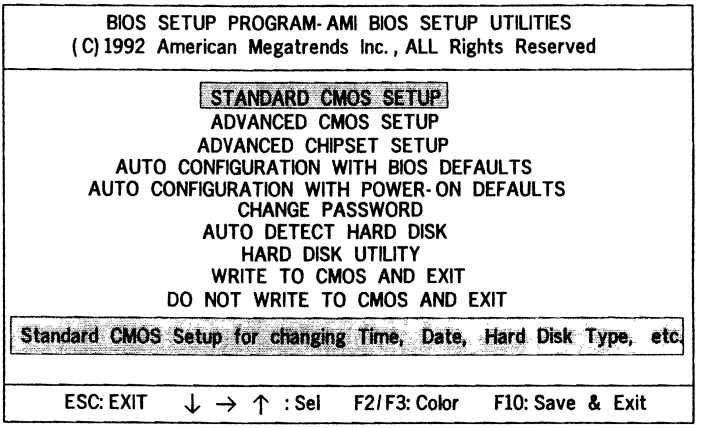
CHAPTER 3 SYSTEM SETUP

AMI BIOS SYSTEM CONFIGURATION SETUP

This section will tell you how to set up the system configurations (CMOS) under the AMI BIOS. After booting the system and testing the memory.

The SETUP program is contained in the system's Read-Only-Memory Rather than on a diskette.

To enter SETUP, press the "DEL" key. The following menu appears:



Please enter "STANDARD CMOS SETUP" to enter the next screen.

The following pages show simple charts and instructions for the CMOS setup.

BIOS SETUP PROGRAM- WARNING INFORMATION
(C) 1992 American Megatrends Inc., All Rights Reserved

Improper Use of Setup may Casuse Problems!!

If System Hangs, Reboot System and Enter Setup by Pressing the <DEL> key

Do any of the following After Entering Setup
(i) Alter Options to make System Work
(ii) Load BIOS Setup Defaults
(iii) Load Power-on Defaults

Hit "ESC" to Stop now, Any other Key to Continue

BIOS SETUP PROGRAM- STANDARD CMOS SETUP
(C) 1992 American Megatrends Inc., All Rights Reserved

Date (mm/date/year) : Sun, Jan 20 1992
Time (hour/min/sec) : 19: 39: 53

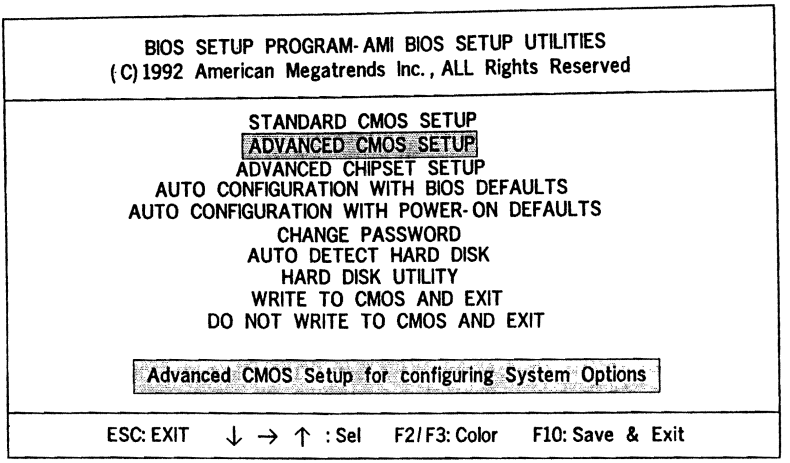
Base memory size: 640 KB
Ext. memory size: 7168 KB

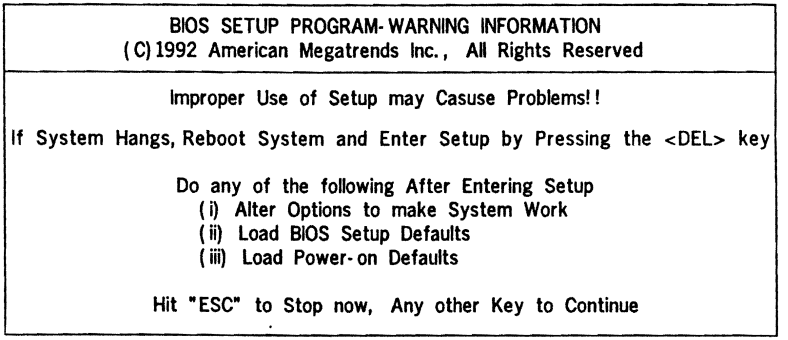
		Cyln	Head	WPcom	LZone	Sect	Size
Hard disk C: type	: 37	615	8	128	615	17	41MB
Hard disk D: type	: Not Installed						
Floppy drive A:	: 1.2 MB, 5 1/4"						
Floppy drive B:	: Not Installed						
Primary display	: Monochrome						
Keyboard	: Installed						

Month : Jan, Feb.....Dec
Date : 01 02 03,.....31
Year : 1901, 1902,.....2099

Sat	Mon	Tue	Wed	Thu	Fri	Sat
29	30	31	1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	1
2	3	4	5	6	7	8

ESC: Exit ↓ → ↑ : Select F2/F3: Color PU/PD: Modify


BIOS SETUP PROGRAM- AMI BIOS SETUP UTILITIES
(C) 1992 American Megatrends Inc., ALL Rights Reserved
STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
AUTO CONFIGURATION WITH POWER-ON DEFAULTS
CHANGE PASSWORD
AUTO DETECT HARD DISK
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT
Advanced CMOS Setup for configuring System Options
ESC: EXIT ↓ → ↑ : Sel F2/F3: Color F10: Save & Exit


BIOS SETUP PROGRAM- WARNING INFORMATION
(C) 1992 American Megatrends Inc., All Rights Reserved
Improper Use of Setup may Casuse Problems!!
If System Hangs, Reboot System and Enter Setup by Pressing the <DEL> key
Do any of the following After Entering Setup
(i) Alter Options to make System Work
(ii) Load BIOS Setup Defaults
(iii) Load Power-on Defaults
Hit "ESC" to Stop now, Any other Key to Continue

BIOS SETUP PROGRAM- WARNING INFORMATION
(C) 1992 American Megatrends Inc., All Rights Reserved

Improper Use of Setup may Casuse Problems!!

If System Hangs, Reboot System and Enter Setup by Pressing the <DEL> key

Do any of the following After Entering Setup
(i) Alter Options to make System Work
(ii) Load BIOS Setup Defaults
(iii) Load Power-on Defaults

Hit "ESC" to Stop now, Any other Key to Continue

BIOS SETUP PROGRAM- ADVANCE CHIPSET SETUP
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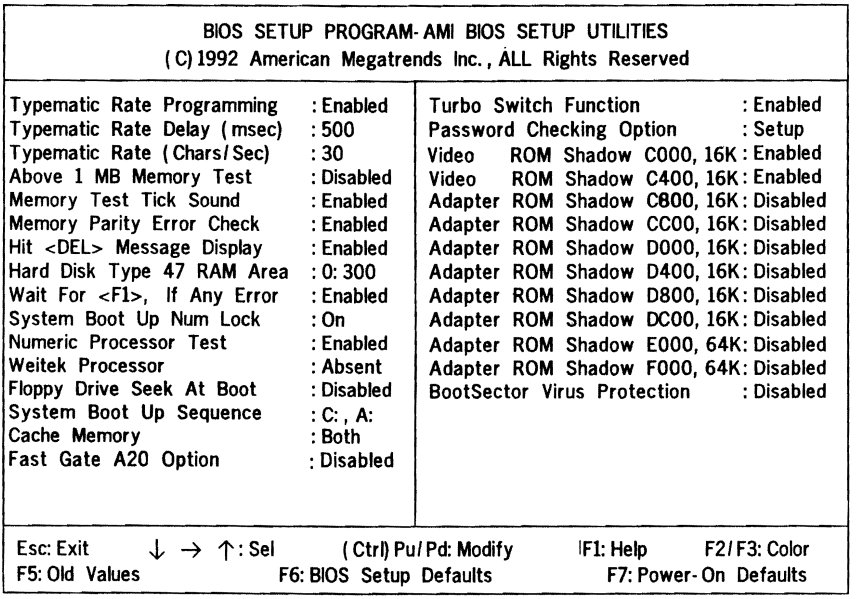
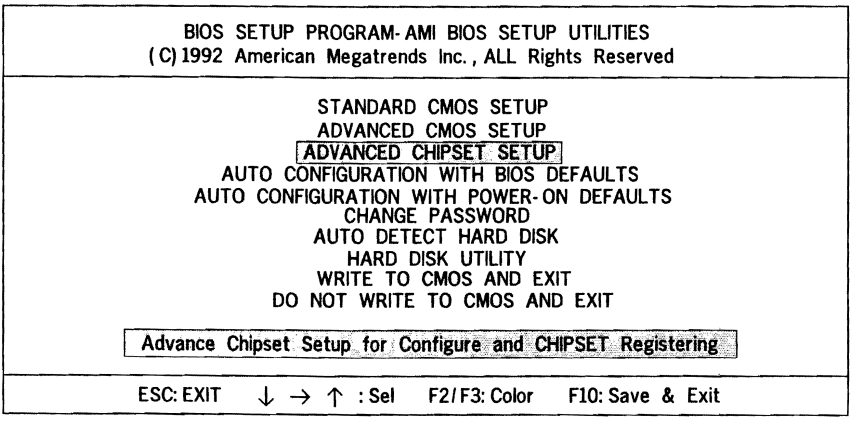
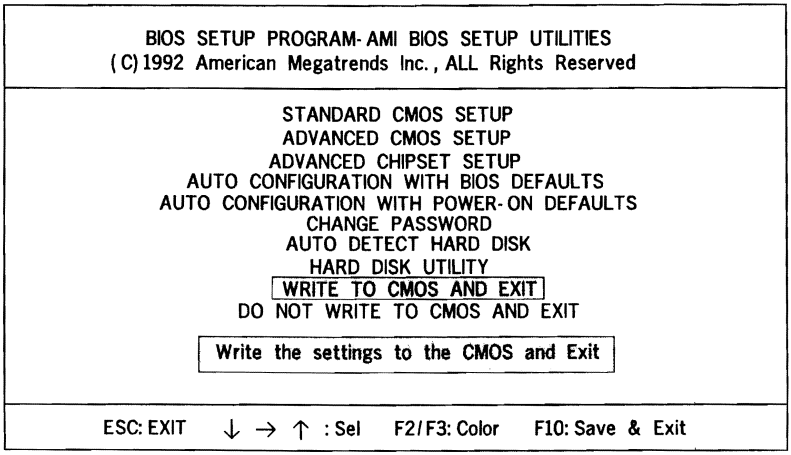
CPU Address Pipeline Mode	:	Disabled	System BIOS Area Cacheable : Disabled
Hidden Refresh	:	Disabled	
CAS Precharge	:	2 CLKs	
Read CAS Pulsewidth	:	3 CLKs	
Write CAS Pulsewidth	:	3 CLKs	
DRAM Post Write	:	Disabled	
512K to 640K DRAM	:	Enabled	
Internal Cache Write Policy	:	Wr-Back	
External Cache Write Policy	:	Wr-Thru	
Cache Read Burst Mode	:	3-3-3-3	
Cache Write Burst Mode	:	4-2-2-2	
DRAM Region A Control Mode	:	Disabled	
DRAM Region A Size	:	512 KB	
DRAM Region A Base Address	:	0KB	
DRAM Region B Control Mode	:	Disabled	
DRAM Region B Size	:	512 KB	
DRAM Region B Base Address	:	0KB	
Video BIOS Area Cacheable	:	Disabled	

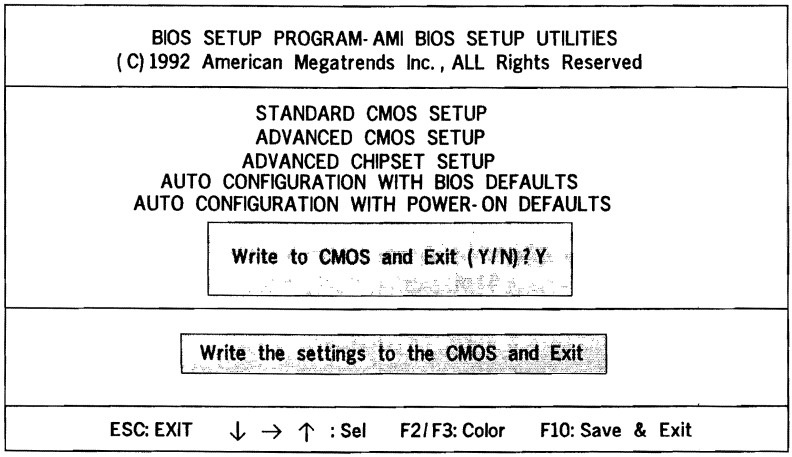
Esc: Exit ↓ → ↑: Sel (Ctrl) Pu/Pd: Modify F1: Help F2/F3: Color
F5: Old Values F6: BIOS Setup Defaults F7: Power-On Defaults


BIOS SETUP PROGRAM- AMI BIOS SETUP UTILITIES
(C) 1992 American Megatrends Inc., ALL Rights Reserved
Typematic Rate Programming : Enabled
Typematic Rate Delay (msec) : 500
Typematic Rate (Chars/ Sec) : 30
Above 1 MB Memory Test : Disabled
Memory Test Tick Sound : Enabled
Memory Parity Error Check : Enabled
Hit <DEL> Message Display : Enabled
Hard Disk Type 47 RAM Area : 0: 300
Wait For <F1>, If Any Error : Enabled
System Boot Up Num Lock : On
Numeric Processor Test : Enabled
Weitek Processor : Absent
Floppy Drive Seek At Boot : Disabled
System Boot Up Sequence : C:, A:
Cache Memory : Both
Fast Gate A20 Option : Disabled
Turbo Switch Function : Enabled
Password Checking Option : Setup
Video ROM Shadow C000, 16K : Enabled
Video ROM Shadow C400, 16K : Enabled
Adapter ROM Shadow C800, 16K : Disabled
Adapter ROM Shadow CC00, 16K : Disabled
Adapter ROM Shadow D000, 16K : Disabled
Adapter ROM Shadow D400, 16K : Disabled
Adapter ROM Shadow D800, 16K : Disabled
Adapter ROM Shadow DC00, 16K : Disabled
Adapter ROM Shadow E000, 64K : Disabled
Adapter ROM Shadow F000, 64K : Disabled
BootSector Virus Protection : Disabled
Esc: Exit ↓ → ↑ : Sel (Ctrl) Pu/ Pd: Modify F1: Help F2/ F3: Color
F5: Old Values F6: BIOS Setup Defaults F7: Power- On Defaults


BIOS SETUP PROGRAM- AMI BIOS SETUP UTILITIES
(C) 1992 American Megatrends Inc., ALL Rights Reserved
STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
AUTO CONFIGURATION WITH POWER- ON DEFAULTS
CHANGE PASSWORD
AUTO DETECT HARD DISK
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT
Advance Chipset Setup for Configure and CHIPSET Registering
ESC: EXIT ↓ → ↑ : Sel F2/ F3: Color F10: Save & Exit

Select this option and press "ENTER" key after CMOS setup is done to aceivate the changes. User is prompted "Write to CMOS and EXIT(Y/N) ? "N". Press "Y" to save the changes and System reboot. Press "N" to go back to the setup program.



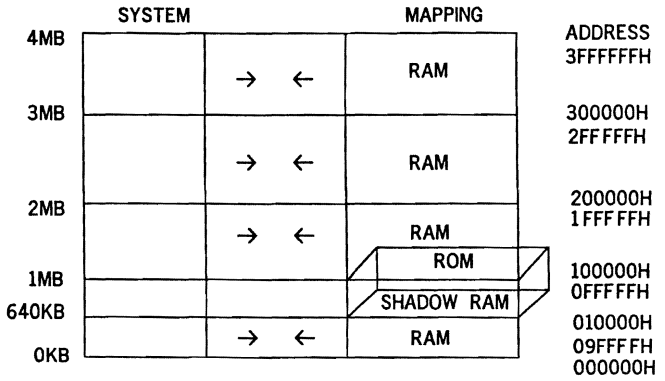


SHADOW RAM

For efficient execution of BIOS, it is prefer able to execute BIOS code through RAM rather than through slower EPROMs. The OPTI-Pentium provides the shadow RAM feature which if enabled allows the BIOS code to be executed from address like BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance of BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benchmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

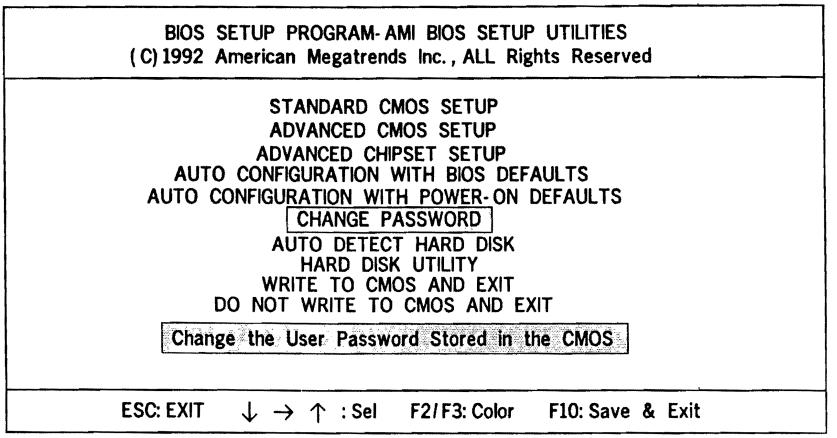
When the Shadow RAM feature is beiing utilized, then the RAM is mapped as shown in Figure 1, overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS,

- FIGURE 1 RAM MAPPING WITH SHADOW RAM (MORE THAN 1MB OF RAM)

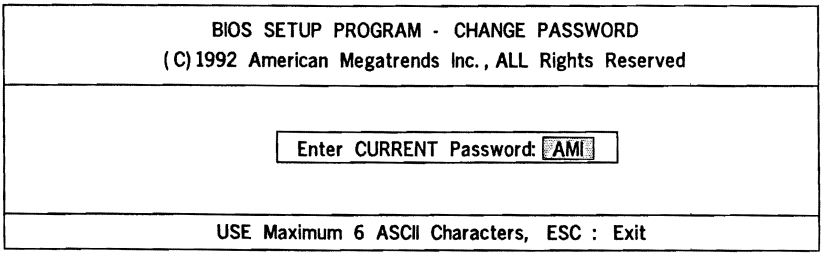


APPENDIX A

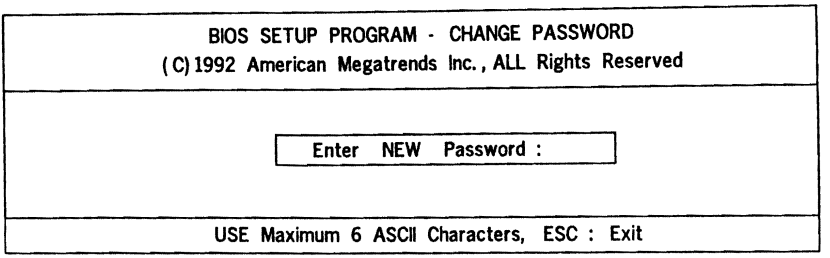
NOTICE : *PLEASE REMEMBER YOUR PASSWORD OF SETTED CHARACTERS! IF KEY IN ERROR PASSWORD THE SYSTEM CAN'T BOOT ON ANY MORE!!*

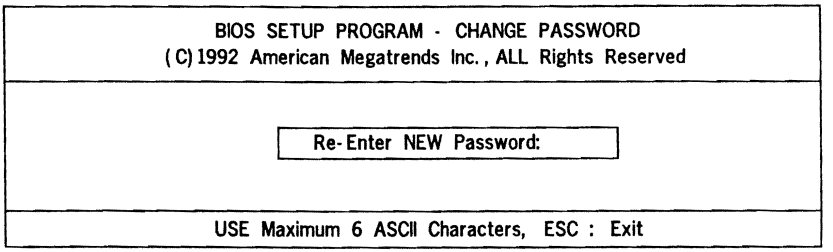


- *(1) PLEASE KEY IN DEFAULT PASSWORD DEFAULT IS "AMI" (FIRST TIME)*
  *(2) IF YOU HAVE SET OWN PASSWORD ALREADY, KEY IN YOUR PASSWORD "*******"*

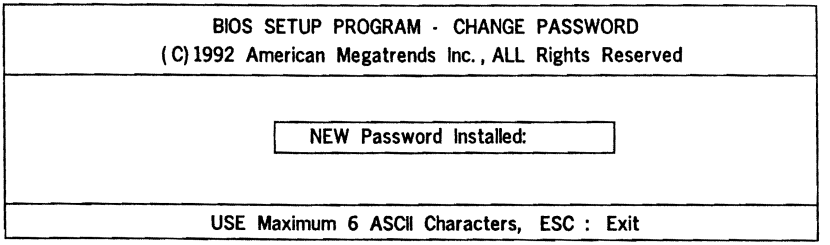


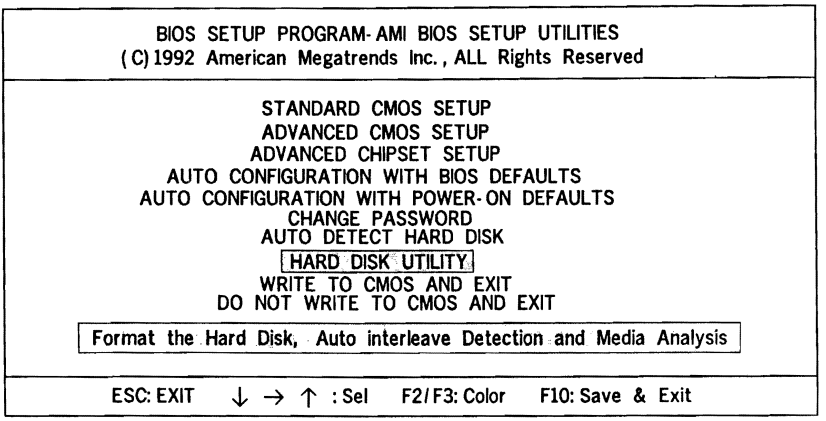
■ *IF YOU WANT TO CHANGE NEW PASSWORD GO TO NEXT SETUP !*

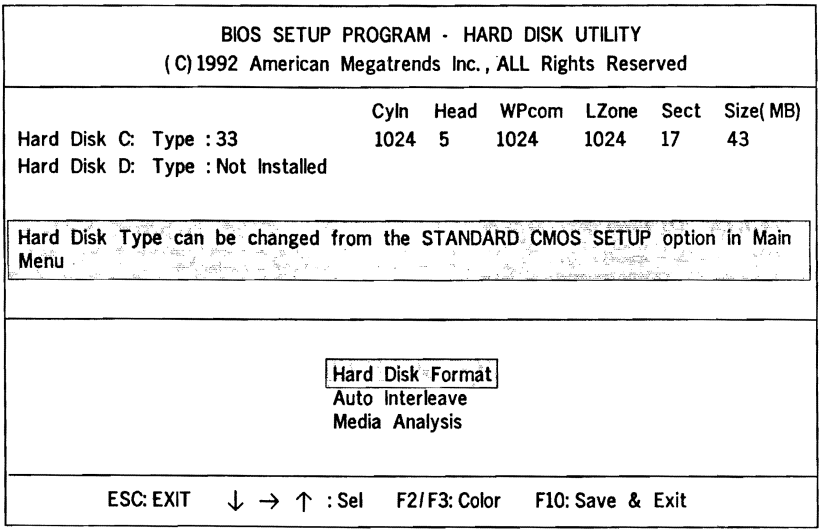


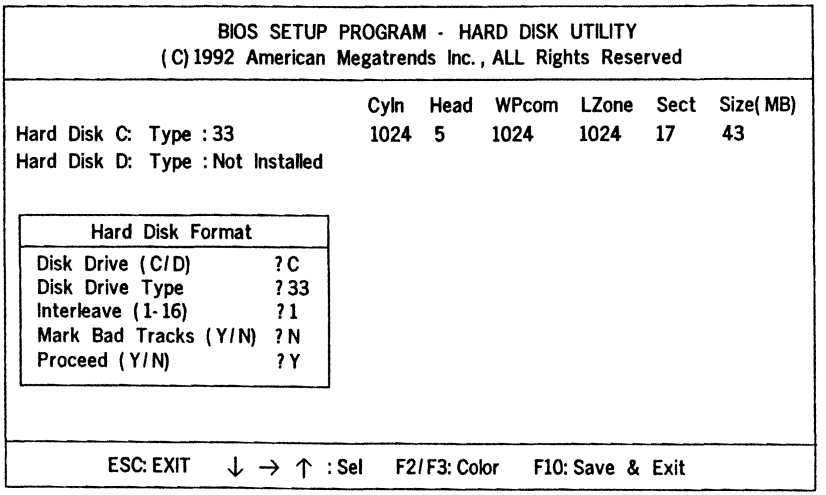


■ *NEXT SCREEN OF MEANING IS YOU HAVE FINISHED PASSWORD SETTINGS! PRESS "ENTER" TO FINAL !*




BIOS SETUP PROGRAM- AMI BIOS SETUP UTILITIES
(C) 1992 American Megatrends Inc., ALL Rights Reserved
STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
AUTO CONFIGURATION WITH POWER-ON DEFAULTS
CHANGE PASSWORD
AUTO DETECT HARD DISK
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT
Format the Hard Disk, Auto interleave Detection and Media Analysis
ESC: EXIT ↓ → ↑ : Sel F2/F3: Color F10: Save & Exit


BIOS SETUP PROGRAM - HARD DISK UTILITY
(C) 1992 American Megatrends Inc., ALL Rights Reserved
Cyln Head WPcom LZone Sect Size(MB)
Hard Disk C: Type : 33 1024 5 1024 1024 17 43
Hard Disk D: Type : Not Installed
Hard Disk Type can be changed from the STANDARD CMOS SETUP option in Main Menu
Hard Disk Format
Auto Interleave
Media Analysis
ESC: EXIT ↓ → ↑ : Sel F2/F3: Color F10: Save & Exit


BIOS SETUP PROGRAM - HARD DISK UTILITY
(C)1992 American Megatrends Inc., ALL Rights Reserved
Cyln Head WPcom LZone Sect Size(MB)
Hard Disk C: Type : 33 1024 5 1024 1024 17 43
Hard Disk D: Type : Not Installed
Hard Disk Format
Disk Drive (C/D) ?C
Disk Drive Type ?33
Interleave (1-16) ?1
Mark Bad Tracks (Y/N) ?N
Proceed (Y/N) ?Y
ESC: EXIT ↓ → ↑ : Sel F2/F3: Color F10: Save & Exit

APPENDIX B

AMI BIOS POST CODES

When the system is powered on, the BIOS will perform diagnostics and initialize all system components, including the video system. All errors found by the BIOS will be put in I/O port 80H. (It's post error code must **INSTALL POST ERROR DEBUG CARD**, just can display it)

POST	DESCRIPTION
01	Processor register test about to start, and NMI to be disabled.
02	NMI is disabled. Power on delay starting
03	Power on delay complete. Any initialization before keyboard BAT is in progeress.
04	Any initialization before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset/power-on
05	Soft reset/power-on determined. Going to enable ROM, i.e. disable shadow RAM/Cache if any.
06	ROM is enabled. Calculating ROM BIOS checksum, and waiting for KB controller input buffer to be free.
07	ROM BIOS checksum passed. KB controller I/B free. Going to issue the BAT command to keyboard controller.
08	BAT command to keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command byte data.
0B	Keyboard controller command byte is written. Going to issue Pin-23, 24 blocking/unblocking command.
0C	Pin-23, 24 of keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register text to be done next.
0E	CMOS shutdown register R/W test passed. Going to calculate CMOS checksum, and update DIAG byte.

0F	CMOS checksum calculation is done. DIAG byte written. CMOS init to begin (If "INIT CMOS IN EVERY BOOT IS SET").
10	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
11	CMOS status register initialised. Going to disable DMA and Interrupt controllers.
12	DMA controller#1, #2, interrupt controller#1, #2 disable. About to disable video display and init port-B.
13	Video display is disabled and port-B is initialized. Chipset init/auto memory detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
16	CH-2 timer test over. 8254 CH-1 timer test to be complete.
17	CH-1 timer test over. 8254 CH-0 timer test to be complete.
18	CH-0 timer test over. About to start memory refresh.
19	Memory Refresh started. Memory refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
1B	Memory Refresh period 30 micro second test complete. Base 64K memory test about to start.
20	Base 64K memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64K sequential data R/W test passed. Any setup before Interrupt vector init about to start.
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch(if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is complete. Going for monochrome mode setting.
29	Monochrome mode setting is done. Going for color mode setting.
2A	Color mode setting is done. About to go for toggle parity before optional ROM test.

2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
2E	Return from processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternated display memory R/W test.
32	Alternate display memory R/W test passed. About to look for the alternate display retrace checking.
33	Video display checking over. Verification of display type with switch setting and actual card to begin.
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message is complete. Going to display the power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the referance string.
3A	Reference string display is over. Going to display the Hit <ESC> message.
3B	Hit <ESC> message displayed. Virtual mode memory test about to start.
40	Preperation for virtual mode test started. Going to vrtify from video memory.
41	Returned after verifying from display memory. Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupt for diagnostics mode.
44	Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory wrap around at 0: 0.
45	Data initizlized. Going to check for memory wrap around at 0: 0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640K memory.

48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4A	Amount of memory above 1M found and verifind. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <ESC> and to clear memory below 1M soft reset.
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size.
4E	Momory test started. (NO SOFT RESET) About to display the first 64K memory test.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memoey test.
50	Memory test below 1M complete. Going to adjust memory size for relocation/ shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1M to follow.
52	Memory test above 1M complete. Going to prepare to go back to real mode.
53	CPU registers are saved including memory size. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area check to be complete.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be checked.
58	BIOS ROM data area check over. Going to clear Hit <ESC> message.
59	Hit <ESC> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.

65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing output buffer, checking for stuck key. About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written. Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Returned from CMOS setup program and screen is cleared. About to do program after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display <WAIT...> message.
8B	<WAIT...> message displayed. About to do Main and Video BIOS shadow.
8C	Main and video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed, mouse check and init to be do next.
8E	Mouse check and initialization complete. Going for hard disk, floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support, hard disk type-47. Going to verify from display memory.

96	Return after verifying from display memory. Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before co-processor test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is complete. Going to check extd keyboard , keyboard ID and num-lock.
9F	Extd keyboard check is done, ID flag set, num-lock on/off, keyboard ID command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft error.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

APPENDIX C

BEEP CODE

During the POST (Power On Self Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to contiune the boot up process. The error messages normally appear on the screen. See Appendix B/C for BIOS Error Messages.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

No. of Beeps Error Message

1. **Refresh Failure**- The memory refresh circuitry of the motherboard is faulty.

2. **Parity Error**- A parity error was detected in the base memory (the first block of 64KB) of the system.

3. **Base 64KB Memory Failure**- A memory failure occured within the first 64KB of memory.

4. **Timer Not Operational**- Timer #1 on the system board has failed to function properly.

5. **Processor Error**- The CPU on the system board has generated an error.

6. **8042-Gate A20 Failure**- The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error message means that the BIOS is not able to switch the CPU into protected mode.

7. **Processor Exception Interrupt Error**- The CPU on the motherboard has generated an exception interrupt.

8. **Display Memory Read/Write Error**- The system video adapter is either missing or its memory is faulty. PLEASE NOTE: This is not a fatal error.

9. **ROM Checksum Error**- The ROM checksum value does not match the value encoded in the BIOS.

10. **CMOS Shutdown Register Read/Write Error**- The shutdown register for the CMOS memory has failed.

RMA FORM

When M/B can't work well, please fill this form to describe related situations. If the space is not enough to use, you can attach another paper.

MODEL: **MODEL NO.:**

HARDWARE:

CPU: Brand_____, Model_____, Speed_____MHz
CO-PROCESSOR: Brand _____, Model_____, Speed_____MHz
SIMM: Brand_____, Speed_____ns, Q'ty_____pcs, Total_____MB
CACHE: Brand_____, Speed_____ns, Total_____K
TAG RAM: Brand_____, Speed_____ns
BIOS DATE CODE:_____
SYSTEM SPEED RUNNING_____MHz
VIDEO CARD: Chip _____, RAM_____, Maker_____VGA Mode
OTHER ADD-ON CARDS:

SOFTWARE:

OPERATION SYSTEM_____VERSION_____
SOFTWARE PROGRAM_____
BIOS SETUP: DRAM wait_____CACHE wait_____
If you change BIOS SETUP, please describe the changes:

<A> ERROR

☐ HANG UP ☐ NO SCREEN ☐ FLOPY R/W ERROR

☐ HARD DISK R/W ERROR ☐ PARITY MEMORY ERROR

☐ OTHER_____

<B> ERROR MESSAGE ON YOUR SCREEN (PLEASE SHOW US CHARACTER)

<C> PROBLEM DESCRIPTION