MOTOROLA POWERPC 603e™ MICROPROCESSOR

The Motorola PowerPC 603e microprocessor (MPC603e) is a low-power implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The PowerPC 603e microprocessor offers workstation-level performance packed into a low-power, low-cost design ideal for desktop computers, notebooks and battery-powered systems, as well as printer and imaging equipment, telecommunications systems, networking and communications infrastructure, industrial controls, and home entertainment and educational devices. Industrial-grade, extended temperature PowerPC 603e microprocessors are available for harsh operating environments. The PowerPC 603e microprocessor is software- and bus-compatible with the PowerPC 740™, PowerPC 750™, and MPC7400 microprocessor families.

Superscalar Microprocessor

The PowerPC 603e microprocessor is a superscalar design capable of issuing three instructions per clock cycle into five independent execution units, including:

- Integer unit
- Load/Store unit
- Floating-point unit
- System register unit
- Branch processing unit

The ability to execute multiple instructions in parallel, to pipeline instructions, and the use of simple instructions with rapid execution times yields maximum efficiency and throughput for PowerPC 603e systems.

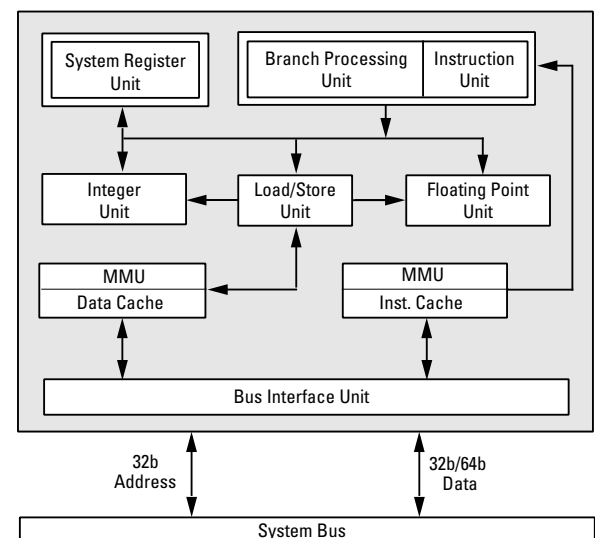## Motorola PowerPC 603e Microprocessor

Product Highlights

The PowerPC 603e microprocessor features a low-power 2.5-volt or 3.3-volt design with three power-saving modes—doze, nap and sleep. These user-programmable modes progressively reduce the power drawn by the processor. The PowerPC 603e microprocessor also uses dynamic power management to selectively activate functional units as they are needed by the executing instructions. Unused functional units enter a low-power state automatically without affecting performance, software execution, or external hardware.
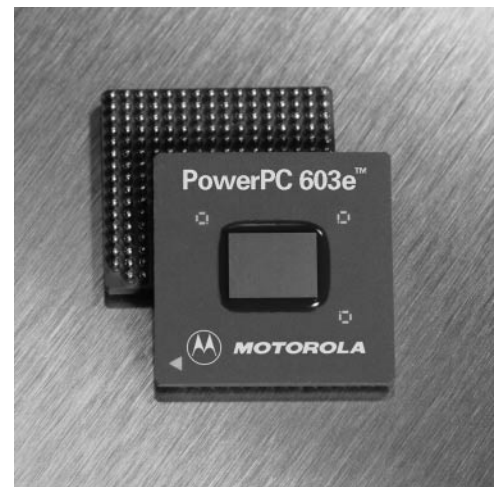
PowerPC 603e Microprocessor Block Diagram

PowerPC™

✻DigitalDNA
From Motorola

Cache and MMU Support

The PowerPC 603e microprocessor has separate 16-Kbyte, physically-addressed instruction and data caches. Both caches are four-way set-associative. The PowerPC 603e microprocessor also contains separate memory management units (MMUs) for instructions and data. The MMUs support 4 Petabytes (2^{52}) of virtual memory and 4 Gigabytes (2^{32}) of physical memory. Access privileges and memory protection are controlled on block or page granularities. Large, 64-entry translation lookaside buffers (TLBs) provide efficient physical address translation and support for demand virtual-memory management on both page- and variable-sized blocks.

Flexible Bus Interface

The PowerPC 603e microprocessor has a selectable 32- or 64-bit data bus and a 32-bit address bus. Support is included for burst, split and pipelined transactions. The interface provides snooping for data cache coherency. The PowerPC 603e microprocessor maintains MEI coherency protocol in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

Contact Information

- Motorola offers user's manuals, application notes and sample code for all of its processors. In addition, local support for these products is also provided. This information can be found at: **http://motorola.com/PowerPC/**

- For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: **Phone: 800-521-6274 or http://motorola.com/semiconductors**

PowerPC 603e CPU Summary

	MPC603e 100-133 MHz	MPC603e 200-300 MHz
CPU Speeds – Internal	100 and 133 MHz	200*, 266 and 300 MHz
CPU Bus Dividers	x1.5, x2, x2.5, x3, x3.5, x4	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6
Bus Interface	64-and 32-bit modes	64-and 32-bit modes
Instructions per Clock	3 (2 + Branch)	3 (2 + Branch)
L1 Cache	16-Kbyte instruction 16-Kbyte data	16-Kbyte instruction 16-Kbyte data
Typical/Maximum Power Dissipation	4.2W/5.3W @ 133 MHz	4.0W/6.0W @ 300 MHz
Die Size	98 mm²	42 mm²
Package	240 CQFP, 255 CBGA	255 CBGA - all: 255 PBGA @200
Process	0.5µ 4LM CMOS	0.29µ 5LM CMOS
Transistors	2.6 million	2.6 million
Voltage	3.3V	3.3V i/o, 2.5V internal
SPECint95 (estimated)	3.9 @ 133 MHz	7.4 @ 300 MHz
SPECfp95 (estimated)	3.1 @133 MHz	6.1 @ 300 MHz
Other Performance	188 MIPS @ 133 MHz	423 MIPS @ 300 MHz
Execution Units	Integer, Floating-Point, Branch, Load/Store, System Register	Integer, Floating-Point, Branch, Load/Store, System Register

*see hardware specifications for operation at lower frequencies

PowerPC 1xx, 6xx and 7xx Part Number Key

MPC	603	R	RX	300	L	C

Product Code
PPC Sample
XPC XC qualified
MPC Qualified

100, 600, or 700 Series Device Number
(106, 107, 603, 740, 745, 750, 755)

Part/Module Modifier
A Alpha (original)
B DGO process
E 603 Enhanced Performance
P Enhanced & Lower Voltage
R 603e in HiP3 process

Package
FE CQFP
RX CBGA w/o lid
PX PBGA w/o lid
ZT PBGA w/lid

Frequency
2-3 digits

Application Modifier
Bus Ratio
C 2:1 (106 only)
D 5:2 (106 only)
L Full spec all modes
-or-
Application Relief
R 105°
T ext. temp. (-40° to 105°)

Revision