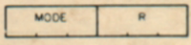
digital

pdp-11

PROGRAMMING CARD

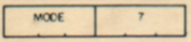
FOR FAMILY OF PDP-11 COMPUTERS

WORD FORMAT:



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) + (1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	–(R)	(R) – (1 or 2); (R) is adrs
5	auto-decr deferred	@–(R)	(R) – 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING: Reg = 7



2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND:

Op Codes

- ▪ = 0 for word/1 for byte
- SS = source field (6 bits)
- DD = destination field (6 bits)
- R = gen register (3 bits), 0 to 7
- XXX = offset (8 bits), +127 to –128
- N = number (3 bits)
- NN = number (6 bits)

Operations

- ( ) = contents of
- s = contents of source
- d = contents of destination
- r = contents of register
- ← = becomes
- X = relative address
- % = register definition

Boolean

- ∧ = AND
- ∨ = inclusive OR
- ⊻ = exclusive OR
- ~ = NOT

Condition Codes

- * = conditionally set/cleared
- – = not affected
- 0 = cleared
- 1 = set

NOTE:

- ▲ = Applies to the 11/35, 11/40, 11/45 & 11/70 computers
- ● = Applies to the 11/45 & 11/70 computers

digital equipment corporation

MAYNARD, MASSACHUSETTS

July 1975

pdp11

NUMERICAL OP CODE LIST:

OP Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07 – 00 00 77	(unused)
00 01 DD	JMP
00 02 OR	RTS
00 02 10 – 00 02 27	(unused)
00 02 3N	SPL
00 02 40	NOP
00 02 41 – 00 02 77	cond codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST

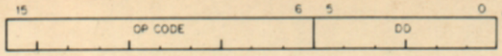
OP Code	Mnemonic
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 65 SS	MFPI
00 66 DD	MTPI
00 67 DD	SXT
00 70 00 – 00 77 77	(unused)
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40 – 07 67 77	(unused)
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC, BHIS
10 34 XXX	BCS, BLO

OP Code	Mnemonic
10 40 00 – 10 43 77	EMT
10 44 00 – 10 47 77	TRAP
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 00 – 10 64 77	(unused)
10 65 SS	MFPD
10 66 DD	MTPD
10 67 00 – 10 77 77	(unused)
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB
17 00 00 – 17 77 77	floating point

TRAP VECTORS:

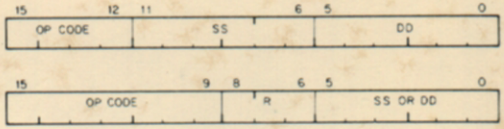
000	(reserved)
004	Time Out & other errors
010	illegal & reserved instr
014	BPT instruction
020	IOT instruction
024	Power Fail
030	EMT instruction
034	TRAP instruction
114	Memory Parity
240	PIRQ, prog int req
244	Floating Point
250	Memory Management

SINGLE OPERAND: OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■ 050DD	clear	0	0	1	0	0
COM(B)	■ 051DD	complement (1's)	~d	*	*	0	1
INC(B)	■ 052DD	increment	d + 1	*	*	*	–
DEC(B)	■ 053DD	decrement	d – 1	*	*	*	–
NEG(B)	■ 054DD	negate (2's compl)	–d	*	*	*	*
TST(B)	■ 057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■ 060DD	rotate right	→C, d	*	*	*	*
ROL(B)	■ 061DD	rotate left	C, d←	*	*	*	*
ASR(B)	■ 062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■ 063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	*	0
Multiple Precision							
ADC(B)	■ 055DD	add carry	d + C	*	*	*	*
SBC(B)	■ 056DD	subtract carry	d – C	*	*	*	*
▲SXT	0067DD	sign extend	0 or –1	–	*	0	–

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst

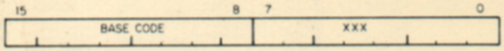


Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■ 1SSDD	move	d ← s	*	*	0	–
CMP(B)	■ 2SSDD	compare	s – d	*	*	*	*
ADD	06SSDD	add	d ← s + d	*	*	*	*
SUB	16SSDD	subtract	d ← d – s	*	*	*	*
Logical							
BIT(B)	■ 3SSDD	bit test (AND)	s ∧ d	*	*	0	–
BIC(B)	■ 4SSDD	bit clear	d ← (~s) ∧ d	*	*	0	–
BIS(B)	■ 5SSDD	bit set (OR)	d ← s ∨ d	*	*	0	–
▲Register							
MUL	070RSS	multiply	r ← r x s	*	*	0	*
DIV	071RSS	divide	r ← r/s	*	*	*	*
ASH	072RSS	shift arithmetically		*	*	*	*
ASHC	073RSS	arith shift combined		*	*	*	*
XOR	074RDD	exclusive OR	d ← r ∨ d	*	*	0	–

BRANCH:

B – – location

If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)
adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	≠ 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	–	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1
Signed Conditional Branches				
BGE	002000	br if greater or eq (to 0)	≥0	N ⊻ V = 0
BLT	002400	br if less than (0)	<0	N ⊻ V = 1
BGT	003000	br if greater than (0)	>0	Z v (N ⊻ V) = 0
BLE	003400	br if less or equal (to 0)	≤0	Z v (N ⊻ V) = 1
Unsigned Conditional Branches				
BHI	101000	branch if higher	>	C v Z = 0
BLOS	101400	branch if lower or same	≤	C v Z = 1
BHIS	103000	branch if higher or same	≥	C = 0
BLO	103400	branch if lower	<	C = 1

JUMP & SUBROUTINE:

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
▲MARK	0064NN	mark	aid in subr return
▲SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) – 1, then if (R) ≠ 0: PC ← Updated PC – (2 x NN)

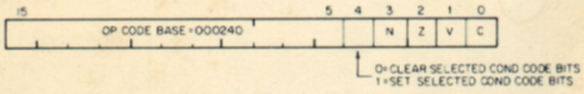
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
▲RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)
●SPL	00023N	set priority level (to N)
▲MFPI	0065SS	move from previous instr space
▲MTPI	0066DD	move to previous instr space
●MFPD	1065SS	move from previous data space
●MTPD	1066DD	move to previous data space

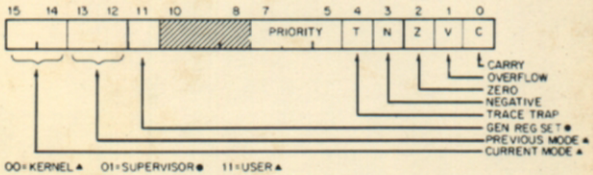
CONDITION CODE OPERATORS:



Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	–	–	–	0
CLV	000242	clear V	–	–	0	–
CLZ	000244	clear Z	–	0	–	–
CLN	000250	clear N	0	–	–	–
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	–	–	–	1
SEV	000262	set V	–	–	1	–
SEZ	000264	set Z	–	1	–	–
SEN	000270	set N	1	–	–	–
SCC	000277	set all cc bits	1	1	1	1

PROCESSOR REGISTER ADDRESSES:

Processor Status Word
PS - 777 776



▲Stack Limit Register — 777 774

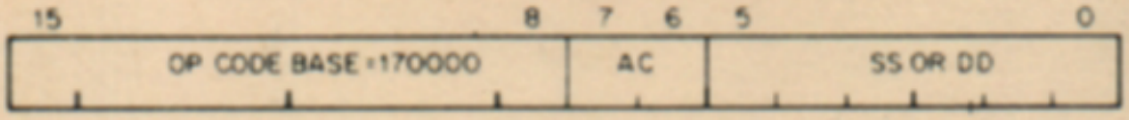
●Program Interrupt Request —777 772

General Registers (console use only)
R0 — 777 700
R1 — 777 701
R2 — 777 702
R3 — 777 703
R4 — 777 704
R5 — 777 705
R6 — 777 706
R7 — 777 707

(not for 11/45)

Console Switches & Display Register — 777 570

PDP-11/45, 11/70 FLOATING POINT PROCESSOR:



Mnemonic	Op Code	Instruction	Operation
CFCC	170000	copy fl cond codes	
SETF	170001	set floating mode	FD ← 0
SETI	170002	set integer mode	FL ← 0
SETD	170011	set fl dbl mode	FD ← 1
SETL	170012	set long integer mode	FL ← 1
LDFPS	1701 src	load FPP prog status	
STFPS	1702 dst	store FPP prog status	
STST	1703 dst	store (exc codes & adrs)	
CLRF, CLRD	1704 fdst	clear floating/double	fdst ← 0
TSTF, TSTD	1705 fdst	test fl/dbl	
ABSF, ABSD	1706 fdst	make absolute fl/dbl	fdst ← |fdst|
NEGF, NEGD	1707 fdst	negate fl/dbl	fdst ← –fdst
MULF, MULD	171 (AC) fsrc	multiply fl/dbl	AC ← AC x fsrc
MODF, MODD	171 (AC + 4) fsrc	multiply & integerize	
ADDF, ADDD	172 (AC) fsrc	add fl/dbl	AC ← AC + fsrc
LDF, LDD	172 (AC + 4) fsrc	load fl/dbl	AC ← fsrc
SUBF, SUBD	173 (AC) fsrc	subtract fl/dbl	AC ← AC — fsrc
CMPF, CMPD	173 (AC + 4) fsrc	compare fl/dbl (to AC)	
STF, STD	174 (AC) fdst	store fl/dbl	fdst ← AC
DIVF, DIVD	174 (AC + 4) fsrc	divide fl/dbl	AC ← AC/fsrc
STEXP	175 (AC) dst	store exponent	
STCFI, STCFL STCDI, STCDL	175 (AC + 4) dst	store & convert fl or dbl to int or long int	
STCFD, STCDF	176 (AC) fdst	store & convert (dbl-fl)	
LDEXP	176 (AC + 4) src	load exponent	
LDCIF, LDCID LDCLF, LDCLD	177 (AC) src	load & convert int or long int to fl or dbl	
LDCDF, LDCFD	177 (AC + 4) fsrc	load & convert (dbl-fl)	

PDP-11/35, 11/40 FLOATING POINT UNIT:

N Z V C

ERT © 1973, 1974, 1975, 1977, 1978 DIGITAL EQUIPMENT CORPORATION

FADD	07500R	floating add	*	*	0	0
FSUB	07501R	floating subtract	*	*	0	0
FMUL	07502R	floating multiply	*	*	0	0
FDIV	07503R	floating divide	*	*	0	0

POWERS OF 2:

n	2^n	n	2^n
0	1	10	1,024
1	2	11	2,048
2	4	12	4,096
3	8	13	8,192
4	16	14	16,384
5	32	15	32,768
6	64	16	65,536
7	128	17	131,072
8	256	18	262,144
9	512	19	524,288

PRINTED IN U.S.A. EH 51046 '78 08A/20 14 50 COPYRIGHT