# SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

## DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

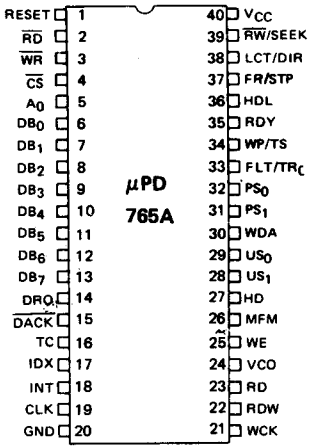
| | | |
|---|---|---|
| Read Data | Scan High or Equal | Write Deleted Data |
| Read ID | Scan Low or Equal | Seek |
| Read Deleted Data | Specify | Recalibrate (Restore to Track 0) |
| Read a Track | Write Data | Sense Interrupt Status |
| Scan Equal | Format a Track | Sense Drive Status |

## FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

## PIN CONFIGURATION

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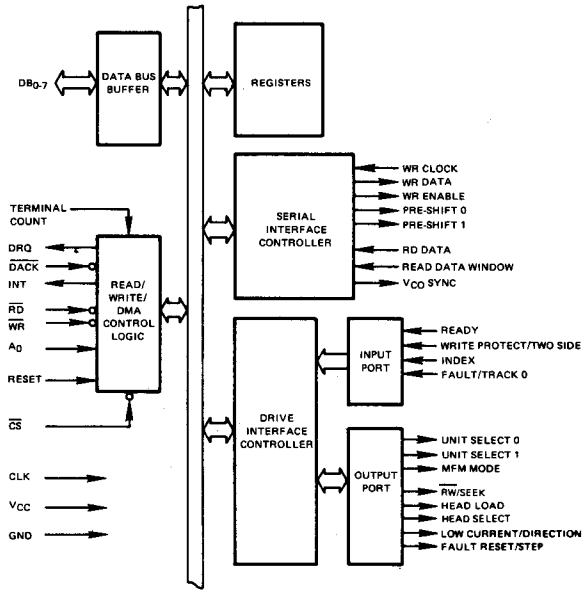
## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Operating Temperature | -10°C to +70°C |
| Storage Temperature | -55°C to +150°C |
| All Output Voltages | -0.5 to +7 Volts |
| All Input Voltages | -0.5 to +7 Volts |
| Supply Voltage $V_{CC}$ | -0.5 to +7 Volts |
| Power Dissipation | 1 Watt |

$T_a$ = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

$T_a$ = -10°C to +70°C; $V_{CC}$ = +5V ± 5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP① | MAX | | |
| Input Low Voltage | $V_{IL}$ | -0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.5 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | $V_{CC}$ | V | $I_{OH}$ = -200 μA |
| Input Low Voltage (CLK + WR Clock) | $V_{IL(\Phi)}$ | -0.5 | | 0.65 | V | |
| Input High Voltage (CLK + WR Clock) | $V_{IH(\Phi)}$ | 2.4 | | $V_{CC}$ + 0.5 | V | |
| $V_{CC}$ Supply Current | $I_{CC}$ | | | 150 | mA | |
| Input Load Current (All Input Pins) | $I_{LI}$ | | | 10 | μA | $V_{IN}$ = $V_{CC}$ |
| | | | | -10 | μA | $V_{IN}$ = 0V |
| High Level Output Leakage Current | $I_{LOH}$ | | | 10 | μA | $V_{OUT}$ = $V_{CC}$ |
| Low Level Output Leakage Current | $I_{LOL}$ | | | -10 | μA | $V_{OUT}$ = +0.45V |

Note: ① Typical values for $T_a$ = 25°C and nominal supply voltage.

## PIN IDENTIFICATION

| PIN NO. | PIN SYMBOL | PIN NAME | INPUT/ OUTPUT | CONNECTION TO | FUNCTION |
|---|---|---|---|---|---|
| 1 | RST | Reset | Input | Processor | Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command. |
| 2 | $\overline{RD}$ | Read | Input (1) | Processor | Control signal for transfer of data from FDC to Data Bus; when "0" (low). |
| 3 | $\overline{WR}$ | Write | Input (1) | Processor | Control signal for transfer of data to FDC via Data Bus, when "0" (low). |
| 4 | $\overline{CS}$ | Chip Select | Input | Processor | IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled. |
| 5 | $A_0$ | Data/Status Reg Select | Input (1) | Processor | Selects Data Reg ($A_0$=1) or Status Reg ($A_0$=0) contents of the FDC to be sent to Data Bus. |
| 6-13 | $DB_0$-$DB_7$ | Data Bus | Input/ (1) Output | Processor | Bi-Directional 8-Bit Data Bus. |
| 14 | DRQ | Data DMA Request | Output | DMA | DMA Request is being made by FDC when DRQ="1". |
| 15 | $\overline{DACK}$ | DMA Acknowledge | Input | DMA | DMA cycle is active when "0" (low) and Controller is performing DMA transfer. |
| 16 | TC | Terminal Count | Input | DMA | Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode. |
| 17 | IDX | Index | Input | FDD | Indicates the beginning of a disk track. |
| 18 | INT | Interrupt | Output | Processor | Interrupt Request Generated by FDC. |
| 19 | CLK | Clock | Input | | Single Phase 8 MHz Squarewave Clock. |
| 20 | GND | Ground | | | D.C. Power Return. |
| 21 | WCK | Write Clock | Input | | Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM. |
| 22 | RDW | Read Data Window | Input | Phase Lock Loop | Generated by PLL, and used to sample data from FDD. |
| 23 | RDD | Read Data | Input | FDD | Read data from FDD, containing clock and data bits. |
| 24 | VCO | VCO Sync | Output | Phase Lock Loop | Inhibits VCO in PLL when "0" (low), enables VCO when "1." |
| 25 | WE | Write Enable | Output | FDD | Enables write data into FDD. |
| 26 | MFM | MFM Mode | Output | Phase Lock Loop | MFM mode when "1," FM mode when "0." |
| 27 | HD | Head Select | Output | FDD | Head 1 selected when "1" (high), Head 0 selected when "0" (low). |
| 28,29 | $US_1$,$US_0$ | Unit Select | Output | FDD | FDD Unit Selected. |
| 30 | WDA | Write Data | Output | FDD | Serial clock and data bits to FDD. |
| 31,32 | $PS_1$,$PS_0$ | Precompensation (pre-shift) | Output | FDD | Write precompensation status during MFM mode. Determines early, late, and normal times. |
| 33 | FLT/$TR_0$ | Fault/Track 0 | Input | FDD | Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode. |
| 34 | WP/TS | Write Protect/ Two-Side | Input | FDD | Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode. |
| 35 | RDY | Ready | Input | FDD | Indicates FDD is ready to send or receive data. |
| 36 | HDL | Head Load | Output | FDD | Command which causes read/write head in FDD to contact diskette. |
| 37 | FR/STP | Fit Reset/Step | Output | FDD | Resets fault F.F. in FDD in Read/Write mode, contains step pulse to move head to another cylinder in Seek mode. |
| 38 | LCT/DIR | Low Current/ Direction | Output | FDD | Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal. |
| 39 | $\overline{RW}$/SEEK | Read Write/SEEK | Output | FDD | When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected. |
| 40 | $V_{CC}$ | +5V | | | DC Power. |

Note: (1) Disabled when CS = 1.

## CAPACITANCE

$T_a = 25°C$; $f_c = 1$ MHz; $V_{CC} = 0V$

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Input Capacitance | $C_{IN(\Phi)}$ | | | 20 | pF | All Pins Except Pin Under Test Tied to AC Ground |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

## AC CHARACTERISTICS

$T_a$ = -10°C to +70°C; $V_{CC}$ = +5V ± 5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP① | MAX | | |
| Clock Period | $\Phi_{CY}$ | 120 | 125 | 500 | ns | |
| Clock Active (High, Low) | $\Phi_0$ | 40 | | | ns | |
| Clock Rise Time | $\Phi_r$ | | | 20 | ns | |
| Clock Fall Time | $\Phi_f$ | | | 20 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓ | $T_{AR}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑ | $T_{RA}$ | 0 | | | ns | |
| $\overline{RD}$ Width | $T_{RR}$ | 250 | | | ns | |
| Data Access Time from $\overline{RD}$ ↓ | $T_{RD}$ | | | 200 | ns | $C_L$ = 100 pf |
| DB to Float Delay Time from $\overline{RD}$ ↑ | $T_{DF}$ | 20 | | 100 | ns | $C_L$ = 100 pF |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓ | $T_{AW}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑ | $T_{WA}$ | 0 | | | ns | |
| $\overline{WR}$ Width | $T_{WW}$ | 250 | | | ns | |
| Data Set Up Time to $\overline{WR}$ ↑ | $T_{DW}$ | 150 | | | ns | |
| Data Hold Time from $\overline{WR}$ ↑ | $T_{WD}$ | 5 | | | ns | |
| INT Delay Time from $\overline{RD}$ ↑ | $T_{RI}$ | | | 500 | ns | |
| INT Delay Time from $\overline{WR}$ ↑ | $T_{WI}$ | | | 500 | ns | |
| DRQ Cycle Time | $T_{MCY}$ | 13 | | | μs | |
| DRQ Delay Time from $\overline{DACK}$ ↓ | $T_{AM}$ | | | 200 | ns | |
| TC Width | $T_{TC}$ | 1 | | | $\Phi$CY | |
| Reset Width | $T_{RST}$ | 14 | | | $\Phi$CY | |
| WCK Cycle Time | $T_{CY}$ | | 2 or 4②<br>1 or 2 | | μs | MFM = 0<br>MFM = 1 |
| WCK Active Time (High) | $T_0$ | 80 | 250 | 350 | ns | |
| WCK Rise Time | $T_r$ | | | 20 | ns | |
| WCK Fall Time | $T_f$ | | | 20 | ns | |
| Pre-Shift Delay Time from WCK ↑ | $T_{CP}$ | 20 | | 100 | ns | |
| WDA Delay Time from WCK ↑ | $T_{CD}$ | 20 | | 100 | ns | |
| RDD Active Time (High) | $T_{RDD}$ | 40 | | | ns | |
| Window Cycle Time | $T_{WCY}$ | | 2.0<br>1.0 | | μs | MFM = 0<br>MFM = 1 |
| Window Hold Time to/from RDD | $T_{RDW}$<br>$T_{WRD}$ | 15 | | | ns | |
| $US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑ | $T_{US}$ | 12 | | | μs | 8 MHz Clock Period |
| SEEK/$\overline{RW}$ Hold Time to LOW CURRENT/DIRECTION ↑ | $T_{SD}$ | 7 | | | μs | |
| LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑ | $T_{DST}$ | 1.0 | | | μs | |
| $US_{0,1}$ Hold Time from FAULT RESET/STEP ↑ | $T_{STU}$ | 5.0 | | | μs | |
| STEP Active Time (High) | $T_{STP}$ | 6.0 | 7.0 | | μs | |
| STEP Cycle Time | $T_{SC}$ | 33 | ③ | ③ | μs | |
| FAULT RESET Active Time (High) | $T_{FR}$ | 8.0 | | 10 | μs | |
| Write Data Width | $T_{WDD}$ | $T_0$-50 | | | ns | |
| $US_{0,1}$ Hold Time After SEEK | $T_{SU}$ | 15 | | | μs | 8 MHz Clock Period |
| Seek Hold Time from DIR | $T_{DS}$ | 30 | | | μs | |
| DIR Hold Time after STEP | $T_{STD}$ | 24 | | | μs | |
| Index Pulse Width | $T_{IDX}$ | 10 | | | $\Phi$CY | |
| $\overline{RD}$ ↓ Delay from DRQ | $T_{MR}$ | 800 | | | ns | 8 MHz Clock Period |
| $\overline{WR}$ ↓ Delay from DRQ | $T_{MW}$ | 250 | | | ns | |
| $\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑ | $T_{MRW}$ | | | 12 | μs | |

Notes: ① Typical values for $T_a$ = 25°C and nominal supply voltage.

② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.

③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

④ For mini-floppy applications, $\Phi_{CY}$ must be 4 mHz.

## AC TEST CONDITION

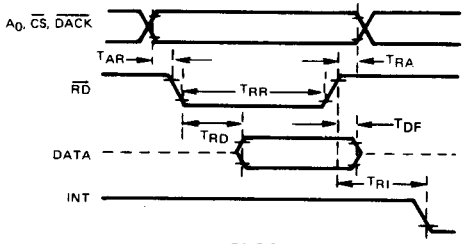

## AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

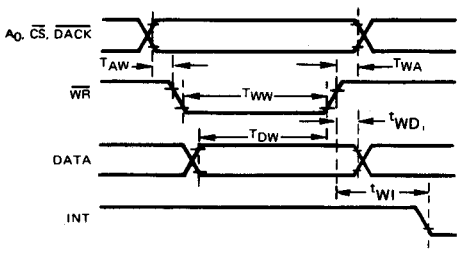
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

## TIMING WAVEFORMS

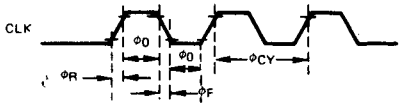
### PROCESSOR READ OPERATION



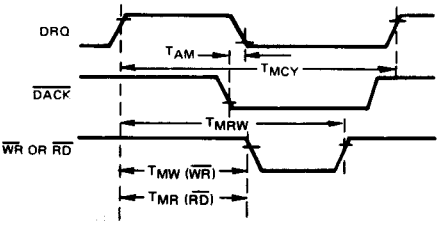

### PROCESSOR WRITE OPERATION



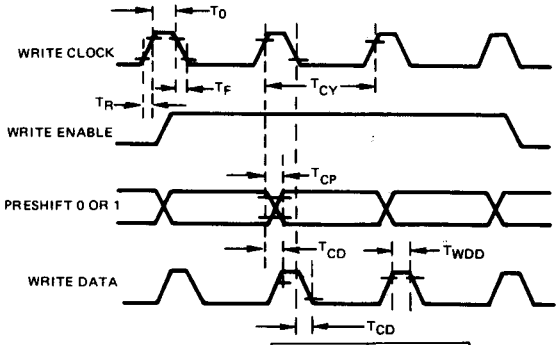

### CLOCK




### DMA OPERATION




### FDD WRITE OPERATION




| | PRESHIFT 0 | PRESHIFT 1 |
|---|---|---|
| NORMAL | 0 | 0 |
| LATE | 0 | 1 |
| EARLY | 1 | 0 |
| INVALID | 1 | 1 |

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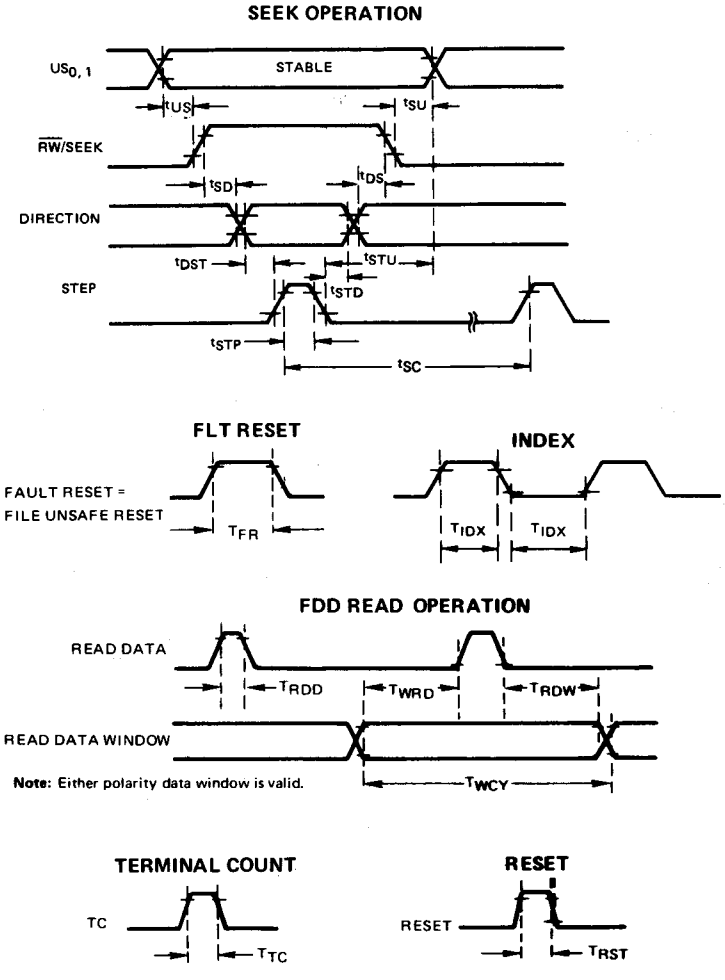
## TIMING WAVEFORMS (CONT.)




## INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and $A_0$ is shown below.

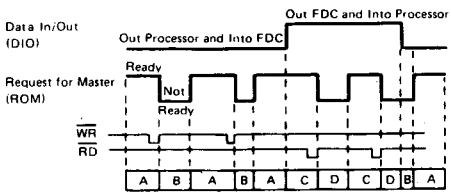
| $A_0$ | $\overline{RD}$ | $\overline{WR}$ | FUNCTION |
|---|---|---|---|
| 0 | 0 | 1 | Read Main Status Register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from Data Register |
| 1 | 1 | 0 | Write into Data Register |

## INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

| BIT NUMBER | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| $DB_0$ | FDD 0 Busy | $D_0B$ | FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_1$ | FDD 1 Busy | $D_1B$ | FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_2$ | FDD 2 Busy | $D_2B$ | FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_3$ | FDD 3 Busy | $D_3B$ | FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_4$ | FDC Busy | CB | A read or write command is in process. FDC will not accept any other command. |
| $DB_5$ | Execution Mode | EXM | This bit is set only during execution phase in non-DMA mode. When $DB_5$ goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation. |
| $DB_6$ | Data Input/Output | DIO | Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register. |
| $DB_7$ | Request for Master | RQM | Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor. |

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when $DB_4$ (FDC Busy) goes low is 12 μs.




Notes: A – Data register ready to be written into by processor
B – Data register not ready to be written into by processor
C – Data register ready for next data byte to be read by the processor
D – Data register not ready for next data byte to be read by processor

## COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

**Command Phase:** The FDC receives all information required to perform a particular operation from the processor.

**Execution Phase:** The FDC performs the operation it was instructed to do.

**Result Phase:** After completion of the operation, status and other housekeeping information are made available to the processor.

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| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 0 | 1 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 1 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 0 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the main-system and FDD |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | SK | 0 | 0 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT. |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ ID** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 0 | 1 | 0 | Commands |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Execution | | | | | | | | | | The first correct ID information on the Cylinder is stored in Data Register |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information read during Execution Phase from Floppy Disk |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **FORMAT A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | N | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | Sectors/Track |
| | W | GPL | | | | | | | | Gap 3 |
| | W | D | | | | | | | | Filler Byte |
| Execution | | | | | | | | | | FDC formats an entire track |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | In this case, the ID information has no meaning |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 0 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

**Note:** ① Symbols used in this table are described at the end of this section.

② $A_0$ should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **SCAN LOW OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN HIGH OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **RECALIBRATE** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | 0 | US1 | US0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 |
| **SENSE INTERRUPT STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command Codes |
| Result | R | STO | | | | | | | | Status information at the end of seek-operation about the FDC |
| | R | PCN | | | | | | | | |
| **SPECIFY** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command Codes |
| | W | SRT | | | | | | HUT | | |
| | W | HLT | | | | | | ND | | |
| **SENSE DRIVE STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Result | R | ST 3 | | | | | | | | Status information about FDD |
| **SEEK** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | NCN | | | | | | | | |
| Execution | | | | | | | | | | Head is positioned over proper Cylinder on Diskette |
| **INVALID** | | | | | | | | | | |
| Command | W | Invalid Codes | | | | | | | | Invalid Command Codes (NoOp – FDC goes into Standby State) |
| Result | R | ST 0 | | | | | | | | ST 0 = 80 (16) |

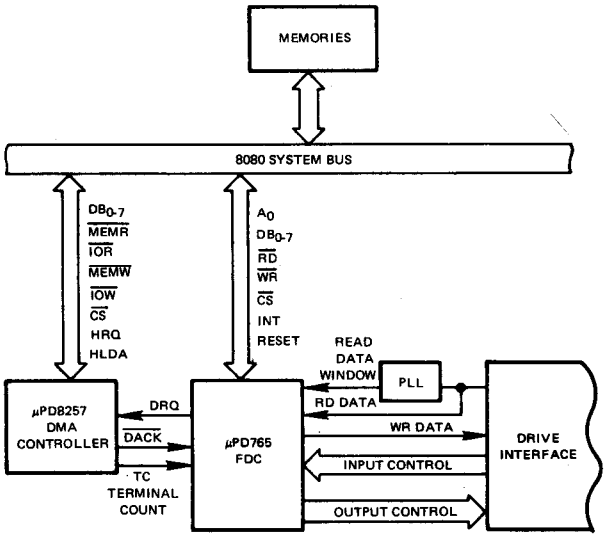
## COMMAND SYMBOL DESCRIPTION

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| $A_0$ | Address Line 0 | $A_0$ controls selection of Main Status Register ($A_0$ = 0) or Data Register ($A_0$ = 1) |
| C | Cylinder Number | C stands for the current/selected Cylinder (track) number 0 through 76 of the medium. |
| D | Data | D stands for the data pattern which is going to be written into a Sector. |
| $D_7$-$D_0$ | Data Bus | 8-bit Data Bus, where $D_7$ stands for a most significant bit, and $D_0$ stands for a least significant bit. |
| DTL | Data Length | When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector. |
| EOT | End of Track | EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT. |
| GPL | Gap Length | GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3. |
| H | Head Address | H stands for head number 0 or 1, as specified in ID field. |
| HD | Head | HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.) |
| HLT | Head Load Time | HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments). |
| HUT | Head Unload Time | HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments). |
| MF | FM or MFM Mode | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT | Multi-Track | If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1. |

## COMMAND SYMBOL DESCRIPTION (CONT.)

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| N | Number | N stands for the number of data bytes written in a Sector. |
| NCN | New Cylinder Number | NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head. |
| ND | Non-DMA Mode | ND stands for operation in the Non-DMA Mode. |
| PCN | Present Cylinder Number | PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time. |
| R | Record | R stands for the Sector number, which will be read or written. |
| R/W | Read/Write | R/W stands for either Read (R) or Write (W) signal. |
| SC | Sector | SC indicates the number of Sectors per Cylinder. |
| SK | Skip | SK stands for Skip Deleted Data Address Mark. |
| SRT | Step Rate Time | SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.). |
| ST 0<br>ST 1<br>ST 2<br>ST 3 | Status 0<br>Status 1<br>Status 2<br>Status 3 | ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command. |
| STP | | During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared. |
| US0, US1 | Unit Select | US stands for a selected drive number 0 or 1. |

## SYSTEM CONFIGURATION



## PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.



## POLLING FEATURE OF THE μPD765

After the Specify command has been sent to the μPD765, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the μPD765 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the μPD765 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

### READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.
The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

| Multi-Track MT | MFM/FM MF | Bytes/Sector N | Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors) | Final Sector Read from Diskette |
|---|---|---|---|---|
| 0 | 0 | 00 | (128) (26) = 3,328 | 26 at Side 0 |
| 0 | 1 | 01 | (256) (26) = 6,656 | or 26 at Side 1 |
| 1 | 0 | 00 | (128) (52) = 6,656 | 26 at Side 1 |
| 1 | 1 | 01 | (256) (52) = 13,312 | |
| 0 | 0 | 01 | (256) (15) = 3,840 | 15 at Side 0 |
| 0 | 1 | 02 | (512) (15) = 7,680 | or 15 at Side 1 |
| 1 | 0 | 01 | (256) (30) = 7,680 | 15 at Side 1 |
| 1 | 1 | 02 | (512) (30) = 15,360 | |
| 0 | 0 | 02 | (512) (8) = 4,096 | 8 at Side 0 |
| 0 | 1 | 03 | (1024) (8) = 8,192 | or 8 at Side 1 |
| 1 | 0 | 02 | (512) (16) = 8,192 | 8 at Side 1 |
| 1 | 1 | 03 | (1024) (16) = 16,384 | |

**Table 1. Transfer Capacity**

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

| MT | HD | Final Sector Transferred to Processor | ID Information at Result Phase | | | |
|---|---|---|---|---|---|---|
| | | | C | H | R | N |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| 1 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | NC | LSB | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | LSB | R = 01 | NC |

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

**WRITE DATA**

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

**WRITE DELETED DATA**

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

**READ DELETED DATA**

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

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**READ A TRACK**

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

**READ ID**

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

**FORMAT A TRACK**

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

| | 8" STANDARD FLOPPY | | | | | 5¼" MINI FLOPPY | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **FORMAT** | **SECTOR SIZE** | **N** | **SC** | **GPL ①** | **GPL ②** | **SECTOR SIZE** | **N** | **SC** | **GPL ①** | **GPL ②** |
| FM Mode | 128 bytes/Sector | 00 | 1A | 07 | 1B | 128 bytes/Sector | 00 | 12 | 07 | 09 |
| | 256 | 01 | 0F | 0E | 2A | 128 | 00 | 10 | 10 | 19 |
| | 512 | 02 | 08 | 1B | 3A | 256 | 01 | 08 | 18 | 30 |
| | 1024 bytes/Sector | 03 | 04 | 47 | 8A | 512 | 02 | 04 | 46 | 87 |
| | 2048 | 04 | 02 | C8 | FF | 1024 | 03 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF | 2048 | 04 | 01 | C8 | FF |
| MFM Mode | 256 | 01 | 1A | 0E | 36 | 256 | 01 | 12 | 0A | 0C |
| | 512 | 02 | 0F | 1B | 54 | 256 | 01 | 10 | 20 | 32 |
| | 1024 | 03 | 08 | 35 | 74 | 512 | 02 | 08 | 2A | 50 |
| | 2048 | 04 | 04 | 99 | FF | 1024 | 03 | 04 | 80 | F0 |
| | 4096 | 05 | 02 | C8 | FF | 2048 | 04 | 02 | C8 | FF |
| | 8192 | 06 | 01 | C8 | FF | 4096 | 05 | 01 | C8 | FF |

**Table 3**

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

③ In MFM mode FDC can not perform a read/write/format operation with 128 bytes/sector. (N = 00)

④ All the values are hexidecimal.

**SCAN COMMANDS**

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidicemial byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

## FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

| COMMAND | STATUS REGISTER 2 | | COMMENTS |
|---|---|---|---|
| | BIT 2 = SN | BIT 3 = SH | |
| Scan Equal | 0 | 1 | $D_{FDD} = D_{Processor}$ |
| | 1 | 0 | $D_{FDD} \neq D_{Processor}$ |
| Scan Low or Equal | 0 | 1 | $D_{FDD} = D_{Processor}$ |
| | 0 | 0 | $D_{FDD} < D_{Processor}$ |
| | 1 | 0 | $D_{FDD} > D_{Processor}$ |
| Scan High or Equal | 0 | 1 | $D_{FDD} = D_{Processor}$ |
| | 0 | 0 | $D_{FDD} > D_{Processor}$ |
| | 1 | 0 | $D_{FDD} < D_{Processor}$ |

**Table 4**

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

### SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $DB_0$-$DB_3$ in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

### RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

### SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, D85 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

| SEEK END | INTERRUPT CODE | | CAUSE |
|---|---|---|---|
| BIT 5 | BIT 6 | BIT 7 | |
| 0 | 1 | 1 | Ready Line changed state, either polarity |
| 1 | 0 | 0 | Normal Termination of Seek or Recalibrate Command |
| 1 | 1 | 0 | Abnormal Termination of Seek or Recalibrate Command |

**Table 5**

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

### SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

### SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

### INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the μPD765 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find a 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| **STATUS REGISTER 0** | | | |
| $D_7$ | Interrupt Code | IC | $D_7 = 0$ and $D_6 = 0$<br>Normal Termination of Command, (NT). Command was completed and properly executed. |
| $D_6$ | | | $D_7 = 0$ and $D_6 = 1$<br>Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed. |
| | | | $D_7 = 1$ and $D_6 = 0$<br>Invalid Command issue, (IC). Command which was issued was never started. |
| | | | $D_7 = 1$ and $D_6 = 1$<br>Abnormal Termination because during command execution the ready signal from FDD changed state. |
| $D_5$ | Seek End | SE | When the FDC completes the SEEK Command, this flag is set to 1 (high). |
| $D_4$ | Equipment Check | EC | If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set. |
| $D_3$ | Not Ready | NR | When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set. |
| $D_2$ | Head Address | HD | This flag is used to indicate the state of the head at Interrupt. |
| $D_1$ | Unit Select 1 | US 1 | These flags are used to indicate a Drive Unit. Number at Interrupt. |
| $D_0$ | Unit Select 0 | US 0 | |
| **STATUS REGISTER 1** | | | |
| $D_7$ | End of Cylinder | EN | When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set. |
| $D_6$ | | | Not used. This bit is always 0 (low). |
| $D_5$ | Data Error | DE | When the FDC detects a CRC error in either the ID field or the data field, this flag is set. |
| $D_4$ | Over Run | OR | If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set. |
| $D_3$ | | | Not used. This bit always 0 (low). |
| $D_2$ | No Data | ND | During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set. |
| | | | During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set. |
| | | | During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set. |

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STATUS REGISTER IDENTIFICATION (CONT.)

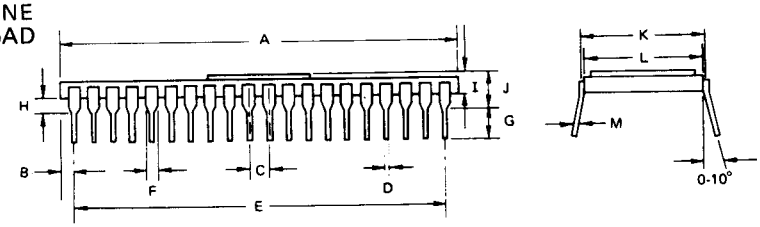
| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| **STATUS REGISTER 1 (CONT.)** | | | |
| $D_1$ | Not Writable | NW | During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set. |
| $D_0$ | Missing Address Mark | MA | If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. |
| | | | If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set. |
| **STATUS REGISTER 2** | | | |
| $D_7$ | | | Not used. This bit is always 0 (low). |
| $D_6$ | Control Mark | CM | During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set. |
| $D_5$ | Data Error in Data Field | DD | If the FDC detects a CRC error in the data field then this flag is set. |
| $D_4$ | Wrong Cylinder | WC | This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set. |
| $D_3$ | Scan Equal Hit | SH | During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set. |
| $D_2$ | Scan Not Satisfied | SN | During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set. |
| $D_1$ | Bad Cylinder | BC | This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set. |
| $D_0$ | Missing Address Mark in Data Field | MD | When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set. |
| **STATUS REGISTER 3** | | | |
| $D_7$ | Fault | FT | This bit is used to indicate the status of the Fault signal from the FDD. |
| $D_6$ | Write Protected | WP | This bit is used to indicate the status of the Write Protected signal from the FDD. |
| $D_5$ | Ready | RY | This bit is used to indicate the status of the Ready signal from the FDD. |
| $D_4$ | Track 0 | T0 | This bit is used to indicate the status of the Track 0 signal from the FDD. |
| $D_3$ | Two Side | TS | This bit is used to indicate the status of the Two Side signal from the FDD. |
| $D_2$ | Head Address | HD | This bit is used to indicate the status of Side Select signal to the FDD. |
| $D_1$ | Unit Select 1 | US 1 | This bit is used to indicate the status of the Unit Select 1 signal to the FDD. |
| $D_0$ | Unit Select 0 | US 0 | This bit is used to indicate the status of the Unit Select 0 signal to the FDD. |

It is suggested that you utilize the following applications notes:

① #8 – for an example of an actual interface, as well as a "theoretical" data separator.

② #10 – for a well documented example of a working phase lock loop.

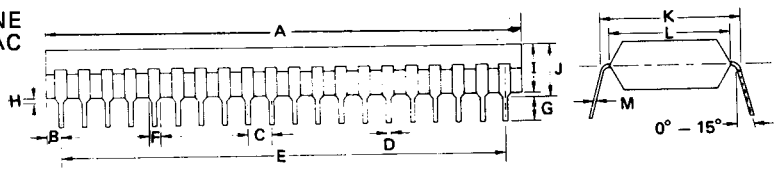
PACKAGE OUTLINE
μPD765AD




Ceramic

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 51.5 MAX | 2.03 MAX |
| B | 1.62 MAX | 0.06 MAX |
| C | 2.54 ± 0.1 | 0.1 ± 0.004 |
| D | 0.5 ± 0.1 | 0.02 ± 0.004 |
| E | 48.26 ± 0.1 | 1.9 ± 0.004 |
| F | 1.02 MIN | 0.04 MIN |
| G | 3.2 MIN | 0.13 MIN |
| H | 1.0 MIN | 0.04 MIN |
| I | 3.5 MAX | 0.14 MAX |
| J | 4.5 MAX | 0.18 MAX |
| K | 15.24 TYP | 0.6 TYP |
| L | 14.93 TYP | 0.59 TYP |
| M | 0.25 ± 0.05 | 0.01 ± 0.0019 |

PACKAGE OUTLINE
μPD765AC




Plastic

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 51.5 MAX | 2.028 MAX |
| B | 1.62 | 0.064 |
| C | 2.54 ± 0.1 | 0.10 ± 0.004 |
| D | 0.5 ± 0.1 | 0.019 ± 0.004 |
| E | 48.26 | 1.9 |
| F | 1.2 MIN | 0.047 MIN |
| G | 2.54 MIN | 0.10 MIN |
| H | 0.5 MIN | 0.019 MIN |
| I | 5.22 MAX | 0.206 MAX |
| J | 5.72 MAX | 0.225 MAX |
| K | 15.24 | 0.600 |
| L | 13.2 | 0.520 |
| M | $0.25^{+0.1}_{0.05}$ | $0.010^{+0.004}_{0.002}$ |

765ADS-REV3-1-82-CAT