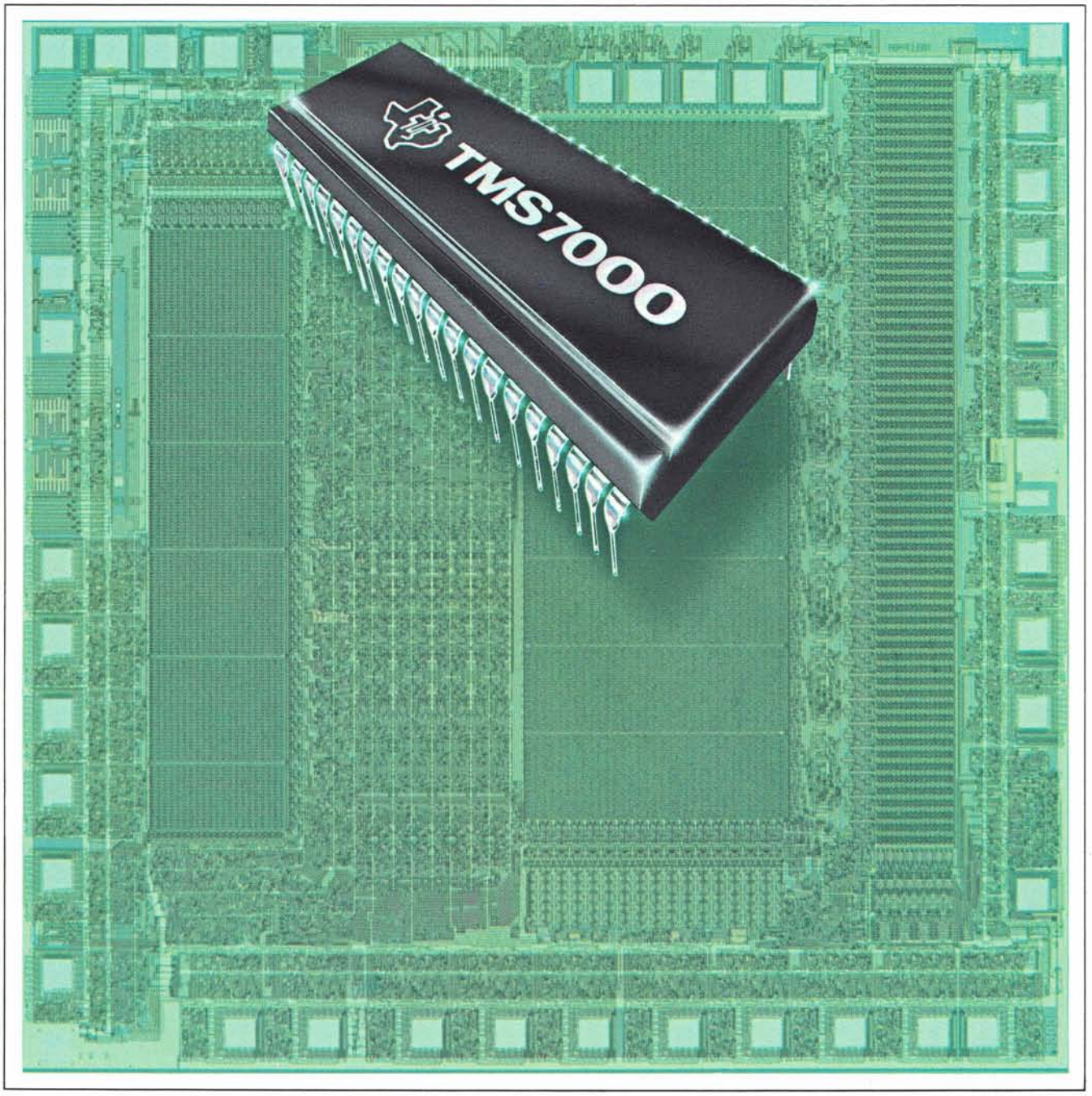
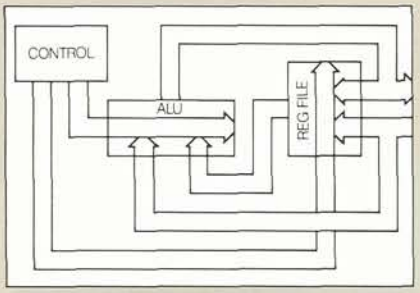
TMS7000 Series

The first microprogrammable 8-bit microcomputer

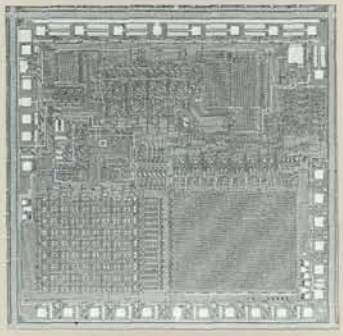
from Texas Instruments



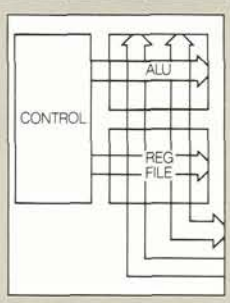
A New Concept in 8-bit Microcomputer Design



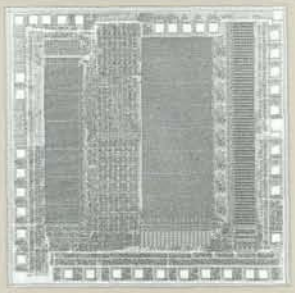
TRADITIONAL DESIGN



TRADITIONAL CHIP (TMS1000)



TMS7000 MICROCOMPUTER STRIP CHIP DESIGN



TMS7000 MICROCOMPUTER STRIP CHIP

The TMS7000 incorporates many of the best features of both memory and register-based microcomputers, and brings many new, unique advantages not available before in a microcomputer of this size.

Beginning with the very layout procedure, designed to reduce interconnection problems of very large scale integration circuits (VLSI), the TMS7000 Series holds many advantages for designers and production people and meets many requirements in design and production.

TI made it the first fully microprogrammable 8-bit microcomputer. This means that the instruction set may be customized to meet specific user application requirements.

Unique Architectural Layout

The unique strip architecture of the TMS7000 Series represents an innovative solution to the on-chip interconnection problem of very complex VLSI devices. The traditional approach to designing a complex microcomputer is to minimize the size of each individual section — control, ALU, and registers, and then use a large amount of random logic to interconnect the sections.

TI took the opposite approach — to eliminate as much random logic as possible by designing individual sections — control, ALU, and registers — for easy interconnections. The net result is a smaller chip for low cost, and a chip that can be easily customized or expanded to add new family members.

For example, the registers for the timer, I/O control, interrupt handling, ALU, etc., are arranged in a strip. This eases future expansion in that the 8-bit additional registers that may be needed, can be added to the strip with the 8-interconnect lines already being available. There is no need for additional registers to be located randomly and then routing interconnect lines all over the bar.

Another concrete example of the strip chips architectural flexibility — TI created the TMS7040 4K ROM version from the TMS7020 2K ROM version without redesigning the chip. The bar design was separated at the memory border and the additional 2K of memory simply inserted alongside the original 2K of memory by the design computer. Likewise, additional features such as more ROM, RAM, or different I/O structures can be added with a minimum of design, resources and time.

TI plans to take advantage of the flexibility of the strip architecture by adding many new devices to the TMS7000 Series in the near future, to offer a broad spectrum of TMS7000 microcomputer devices to meet a wide range of different user requirements.

Unique Microprogrammability Capability

Since a control ROM has replaced random logic for defining the instruction execution sequence, the original TI instruction set can be modified simply by replacing original TI instructions with new user-defined instructions.

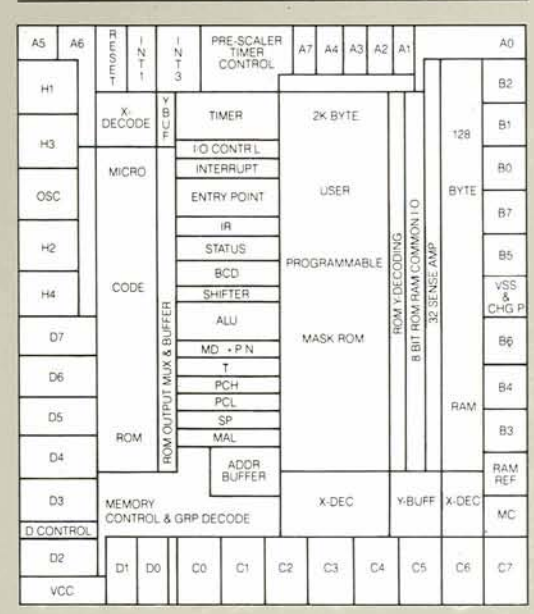
In some user applications, this microprogramming option will enhance the TMS7000 Series microcomputers' performance. By combining or modifying existing micro-instruction execution sequences to perform certain unique, repetitive tasks or sub-routines in less instruction clock cycles, the throughput or "speed" of the microcomputer in the user's application is clearly enhanced.

Another advantage of microprogramming is a more efficient use of the limited on-chip program memory. By combining or modifying the standard micro-instruction execution sequences for certain unique repetitive tasks or subroutines, total application programs may require fewer steps, and less-on-chip program memory.

Microprogramming could also potentially provide increased system security for TMS7000 Series users operating in very competitive business environments. Duplication of a system implemented on a user-defined unique instruction set for the TMS7000 Series microcomputer would be difficult.

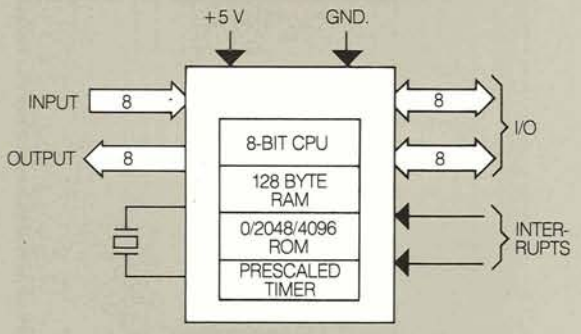
Thus, the net result of the strip architecture of the TMS7000 Series is the availability of a powerful and efficient 8-bit microcomputer at a cost level comparable with many 4-bit microcomputers.

TMS 7020 MICROCOMPUTER BAR PLAN

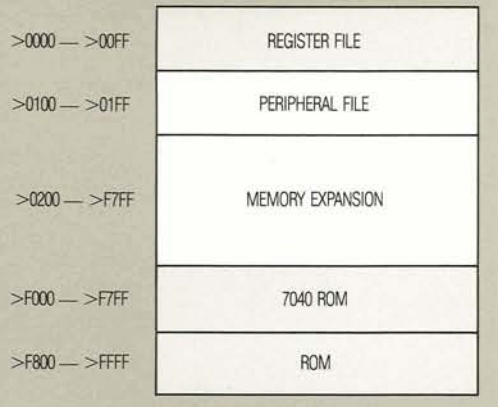


TMS7000 Series Features

TMS7000 SERIES FUNCTIONS



TMS7000 SERIES MEMORY CAPABILITY



The TMS7000, TMS7020 and TMS7040 are the first members of the series with 0, 2048 and 4096 bytes respectively of on-chip ROM. Each offers these outstanding features:

- 8-bit instruction data word
- Instruction set includes 8-bit multiply, BCD add and BCD subtract
- 128 bytes of on-chip RAM
- 0/2048/4096 bytes of on-chip mask programmable ROM
- Program execution from RAM or ROM
- 5-memory expansion modes
- On-chip timer event counter with capture latch
- 32 bits of on-chip I/O
- 3 prioritized interrupts, plus RESET
- 256 byte peripheral I/O file
- 64K byte memory address space
- 5-volt NMOS technology
- 40-pin, 600-mil DIP

Powerful Instruction Set

The TMS7000 Series Standard Instruction Set supports sixty-one distinct, powerful instructions that increase programming efficiency and reduce programming time.

The TMS7000 Series supports single instruction I/O operations on bit fields from 1-8 bits. These powerful I/O instructions allow logical operator manipulation of bit fields without moving I/O data into or out of accumulator registers. This feature increases the flexibility and efficiency of control-oriented programs.

The TMS7000 Series Instruction Set has a unique, powerful "bit test and jump" feature that functions on both I/O and memory data. This provides efficient branching and looping capabilities. Special decrement and jump if non-zero instructions simplify the coding of interactive algorithms.

The TMS7000 Series has a powerful set of arithmetic instructions which set the series apart from other microcomputer systems. Arithmetic operations can be performed on both binary and BCD numbers. Single and multiple precision operations are also available for greater accuracy. Operations include decimal add with carry (DAC) which performs fully corrected additions on two packed BCD bytes, and a companion decimal subtract with borrow (DSB) which performs a similar function for subtract functions. These operations make the TMS7000 Series ideal for point-of-sale terminals.

Another powerful instruction is the 8 x 8 multiply. The TMS7000 Series can perform this unsigned multiply in just 10.8 microseconds with a 8 MHz crystal frequency. This is far superior to software emulation which typically requires 150-200 microseconds to perform.

8-BIT MICROCOMPUTER BENCHMARKS				
PROCESSOR	TMS7000	Z8	8051	6801
CLOCK RATE — MHz	8	8	12	4
BENCHMARKS				
BINARY ADDITION (μs)	4	3	6	13
BCD ADDITION (μs)	6	12	12	22
BLOCK MOVE (μs)	1112	1785	3307	4584
TABLE SEARCH (μs)	283	544	326	645
BINARY TO BCD (μs)	184	236	229	650
BCD TO BINARY (μs)	55	63	46	130
BIT I/O (μs)	13	15	10	33
TOTAL (μs)	1657	2658	3936	6077
RELATIVE PERFORMANCE	1.00	0.62	0.42	0.27
REQUIRED MEMORY SPACE (BYTES)				
	TMS7000	Z8	8051	6801
BINARY ADDITION	4	4	7	6
BCD ADDITION	5	14	14	14
BLOCK MOVE	10	20	33	27
TABLE SEARCH	11	7	20	14
BINARY TO BCD	16	19	23	30
BCD TO BINARY	44	82	50	66
BIT I/O	15	16	17	23
TOTAL	105	162	164	180
RELATIVE EFFICIENCY	1.00	0.65	0.64	0.58

*5 MHz and 8 MHz parts are available.

TMS7000 INSTRUCTION EXECUTION TIMES

INSTRUCTION	MIN-MAX (uS)	NOTES
ADC	2.0-4.0	2,3
ADD	2.0-4.0	2,3
AND	2.0-4.0	2,3
ANDP	3.6-4.4	2,4
BTJO	2.8-4.8	2,3
BTJOP	4.0-4.4	2,4
BTJZ	2.8-4.8	2,3
BTJZP	4.0-4.8	2,4
BR	3.6-4.8	5,6
CALL	5.2-8.4	5,6
CLR	2.0-2.8	2,3
CLRC	2.0	—
CMP	2.0-4.0	2,3
CMPA	4.4-5.6	5,6
DAC	2.8-4.8	2,3
DEC	2.0-2.8	2,3
DECD	3.6-4.4	2,3
DINT	2.0	—
DJNZ	2.8-3.6	2,3
DSB	4.0-4.8	2,3
EINT	2.0	—
IDLE	2.4	—
INC	2.0-2.8	2,3
INV	2.0-2.8	2,3
JMP	2.0-2.8	7
LDA	4.0-5.2	5,6
LDSP	2.0	—
MOV	2.0-4.0	2,3
MOVD	5.2-8.4	3,6
MOVP	3.2-4.4	2,4
MPY	17.2-19.2	2,3
NOP	1.6	—
OR	2.0-4.0	2,3
ORP	3.6-4.4	2,4
POP	2.4-3.2	2,3
PUSH	2.4-3.2	2,3
RETI	3.6	—
RETS	2.8	—
RL	2.0-2.8	2,3
RLC	2.0-2.8	2,3
RR	2.0-2.8	2,3
RRC	2.0-2.8	2,3
SBB	2.0-4.0	2,3
SETC	2.4	—
STA	4.0-5.2	5,6
STSP	2.4	—
SUB	2.0-4.0	2,3
SWAP	3.2-4.0	2,3
TRAP	5.6	—
TSTA	2.4	—
TSTB	2.0	—
XCHB	2.4-3.2	2,3
XOR	2.0-4.0	2,3
XORP	3.6-4.0	2,4

TABLE OF INSTRUCTION EXECUTION TIMES — NOTES

1. THE TIMES ARE BASED ON A CLOCK FREQUENCY OF 5 MHZ.*
2. THE MINIMUM EXECUTION TIME REPRESENTS THE TIME FOR AN A/B REGISTER TRANSFER.
3. THE MAXIMUM EXECUTION TIME REPRESENTS THE TIME FOR A REGISTER FILE TRANSFER.
4. THE MAXIMUM EXECUTION TIME REPRESENTS THE TIME FOR AN IMMEDIATE OPERAND TRANSFER.
5. THE MINIMUM EXECUTION TIME REPRESENTS THE TIME FOR INDIRECT REGISTER FILE TRANSFER.
6. THE MAXIMUM EXECUTION TIME REPRESENTS THE TIME FOR INDEXED GENERAL MEMORY TRANSFER.
7. THE MINIMUM EXECUTION TIME REPRESENTS THE TIME FOR AN UNCONDITIONAL JUMP TO OCCUR, WHILE THE MAXIMUM EXECUTION REPRESENTS THE TIME FOR A CONDITIONAL JUMP TO OCCUR.

TMS7000 Program Flexibility

TMS7000 SERIES ADDRESSING MODES
A REGISTER
B REGISTER
REGISTER FILE
REGISTER FILE INDIRECT
DIRECT
INDEXED
IMMEDIATE
PC RELATIVE
PERIPHERAL FILE (I/O INSTRUCTIONS)

Nine basic addressing modes provide programming flexibility and easy data management. Additionally, the Move Double (MOVD) instruction allows 16-bit addresses to be efficiently manipulated.

The machine state is constantly maintained in three hardware registers: the program counter, status register, and stack pointer. All RAM bytes (128) are addressable as working registers. Therefore, the register contents do not have to be saved on the stack when transferring control to subroutines or interrupts as most other microcomputers must do. The contents may, however, be saved on the stack if required. Parameters may be passed to subroutines via the MLP's RAM resident stack, or through dedicated registers.

Vectored interrupt overhead involves saving only the current program counter and the status register on the stack. The status register may be separately saved or restored from the stack in a single operation. The stack pointer may also be saved or loaded with the program for flexibility of RAM register allocation and segmentation.

The TMS7000 Series allows reduction of both total instruction lengths and execution times. First, by pre-designating R0 and R1 as the A and B registers, any operation involving either of these two registers has the appropriate register number encoded into the op-code. Second, implementation of the subroutine trap vectors allows designating 23 addresses as subroutine destinations. Invocation of the subroutine via the trap is then a single byte instruction.

TMS7000 Performance: Versatile, Powerful and Fast

Standard Instruction Set Summary

The performance advantages of the TMS7000 result from the combination of the versatile instruction set and a micro architecture that provides efficient instruction implementation.

The implementation of the on-chip 128 byte memory resident register file increases program efficiency by providing an 8-bit address for program variables in lieu of 16-bit addresses for general memory accesses. This provides efficient use of program memory as well as increasing execution time. On-chip program memory capitalizes on the performance advantages of on-chip memory through fast instruction acquisition and execution.

TMS7000 SERIES INSTRUCTION SET

MNEMONIC	MEANING
SINGLE OPERAND INSTRUCTIONS	
CLR	CLEAR OPERAND
DEC	DECREMENT
DECD	DECREMENT DOUBLE
INC	INCREMENT
INV	INVERT
POP	POP FROM STACK
PUSH	PUSH ON STACK
RL	ROTATE LEFT
RLC	ROTATE LEFT THROUGH CARRY
RR	ROTATE RIGHT
RRC	ROTATE RIGHT THROUGH CARRY
XCHB	EXCHANGE WITH B REGISTER
DUAL OPERAND INSTRUCTIONS	
ADC	ADD WITH CARRY
ADD	ADD BYTES
AND	AND BYTES
ANDP	AND PERIPHERAL FILE
CMP	COMPARE
DAC	DECIMAL ADD W/CARRY
DSB	DECIMAL SUBTRACT W/BORROW
MOV	MOVE
MOVD	MOVE DOUBLE
MOVP	MOVE TO/FROM PF (PERIPHERAL FILE)
MPY	MULTIPLY
OR	OR
ORP	OR PERIPHERAL FILE
SBB	SUBTRACT WITH BORROW
SUB	SUBTRACT BYTES
XOR	EXCLUSIVE OR
XORP	EXCLUSIVE OR PF
EXTENDED INSTRUCTIONS	
BR	BRANCH
CMPA	COMPARE TO A REGISTER
LDA	LOAD A REGISTER
STA	STORE A REGISTER
JUMP INSTRUCTIONS	
BTJO	BIT TEST JUMP IF ONE
BTJOP	BIT TEST JUMP IF ONE-PF
BTJZ	BIT TEST JUMP IF ZERO
BTJZP	BIT TEST JUMP IF ZERO PF
DJNZ	DEC. REG. JUMP NON-ZERO
JMP	JUMP UNCONDITIONAL
JC/JHS	JUMP IF CARRY SET/ JUMP IF HIGHER OR SAME
JN/JLT	JUMP IF NEGATIVE/ JUMP IF LESS THAN
JNC/JL	JUMP IF NO CARRY/ JUMP IF LOWER
JNZ/JNE	JUMP IF NOT ZERO/ JUMP IF NOT EQUAL
JP/JGT	JUMP IF POSITIVE/ JUMP IF GREATER THAN
JPZ/JGE	JUMP IF POS. OR ZERO/ JUMP IF GREATER OR EQUAL
JZ/JEQ	JUMP IF ZERO/JUMP IF EQUAL TO
CONTROL INSTRUCTIONS	
CLRC	CLEAR CARRY BIT
DINT	DISABLE INTERRUPTS
EINT	ENABLE INTERRUPTS
IDLE	IDLE UNTIL INTERRUPT
LDSP	LOAD STACK POINTER
NOP	NO OPERATION
SETC	SET CARRY
STSP	STORE STACK POINTER
SWAP	SWAP NIBBLES
TSTA	TEST A REGISTER
TSTB	TEST B REGISTER
SUBROUTINE INSTRUCTIONS	
CALL	CALL SUBROUTINE
RETI	RETURN FROM INTERRUPT
RETS	RETURN FROM SUBROUTINE
TRAP 0	TRAP TO SUBROUTINE
•	" " "
•	" " "
•	" " "
TRAP 23	" " "

Advanced Architecture for Advanced I/O Capability

I/O Flexibility

The TMS7000 Series offers the capability of four 8-bit input/output ports and the ability to configure them through the use of five expansion modes. These modes give the TMS7000 Series the flexibility to trade-off pins of dedicated I/O for off-chip peripheral and memory expansion.

The system emulator mode supports an in-circuit emulator. In this mode, all on-chip ROM and I/O is disabled and removed from the memory map, allowing inexpensive configuration of emulator systems.

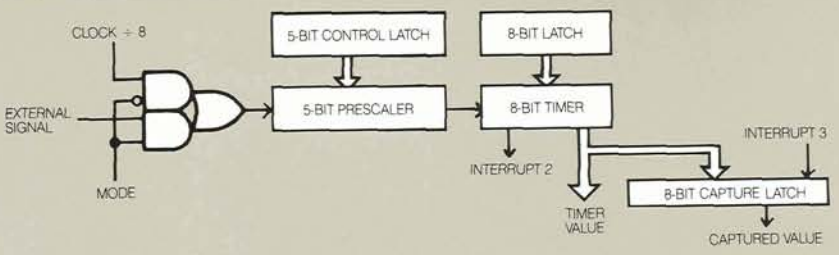
A key feature of the TMS7000 Series is the peripheral file, a 256 byte block of addresses (>0100 to >01FF) which references all of the I/O control and I//O data registers of the chip. Six instructions are dedicated to I/O port data manipulation, providing the bit and byte I/O manipulation required for control applications. Additionally, the I/O ports can be accessed with general extended memory addressing instructions.

Powerful Timer

The on-chip 8-bit timer provides flexibility in system timing tasks with the addition of a 5-bit prescaler driven by either the internal clock or by an external source for event counting. The 5-bit prescaler allows a pre-divide of one to thirty-two to be programmed for optimum resolution for two specific applications. When the 8-bit timer itself decrements through zero, a level 2 interrupt request is issued. In addition, a powerful timer initialization feature allows the timer to be synchronized with other system events.

The capture latch is another powerful feature of the on-chip timer. The occurrence of a level 3 interrupt loads the capture latch with the contents of the timer. Thus, a precise measurement of the time the interrupt occurred is available. This capability is especially valuable when the external event occurs while the processor is servicing a higher-priority interrupt. Tasks such as pulse-width measurement are accommodated with a minimum of external circuitry.

8-BIT TIMER WITH CAPTURE LATCH



TMS7000 Series Memory Expansion Modes

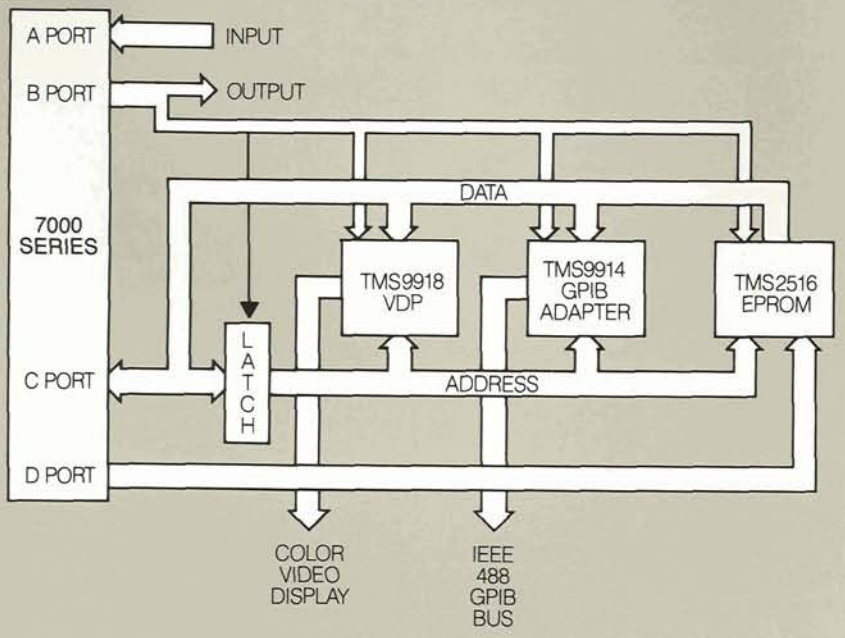
The five memory expansion modes give the TMS7000 Series outstanding flexibility for handling a wide range of different applications. The TMS7020 or TMS7040 can operate as stand-alone single-chip microcomputers when in the *Single-chip mode*. The user has the option of emphasizing either external, peripheral or memory expansion for more complex applications by placing the TMS7020 or TMS7040 in the *Peripheral Expansion mode* or *Memory Expansion mode* respectively. The TMS7000, TMS7020, and TMS7040 can be configured to operate as a ROM-less microcomputer when placed in the *Microprocessor mode*. And finally, the TMS7000, TMS7020, and TMS7040 can be configured in the special *System Emulator mode* to facilitate development of new TMS7000 systems. The following table summarizes the five expansion modes.

MEMORY EXPANSION MODES AND AVAILABILITY

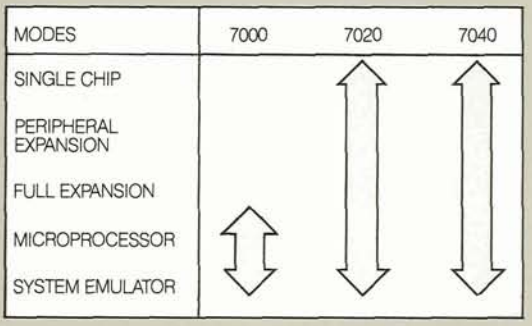
EXPANSION MODES SUMMARY				
EXPANSION MODE	ON-CHIP RAM BYTES	ON-CHIP ROM BYTES	ON-CHIP I/O LINES	OFF-CHIP MEMORY BYTES
		7020/7040	7020/7040	7020/7040
MICROCOMPUTER	128	2048/4096	32	0
PERIPHERAL EXPANSION	128	2048/4096	20	246
FULL EXPANSION	128	2048/4096	12	63224/61176
MICROPROCESSOR*	128	0	12	65272
SYSTEM EMULATOR*	128	0	0	65280

*Also supported by the TMS7000

TMS7000 SERIES
FULL EXPANSION MODE APPLICATION EXAMPLE



TMS7000 SERIES
MEMORY EXPANSION MODES & AVAILABILITY



TMS7000 Series Design Support

The different software and hardware development tools to maximize software productivity for TMS7000 Series users are summarized below:

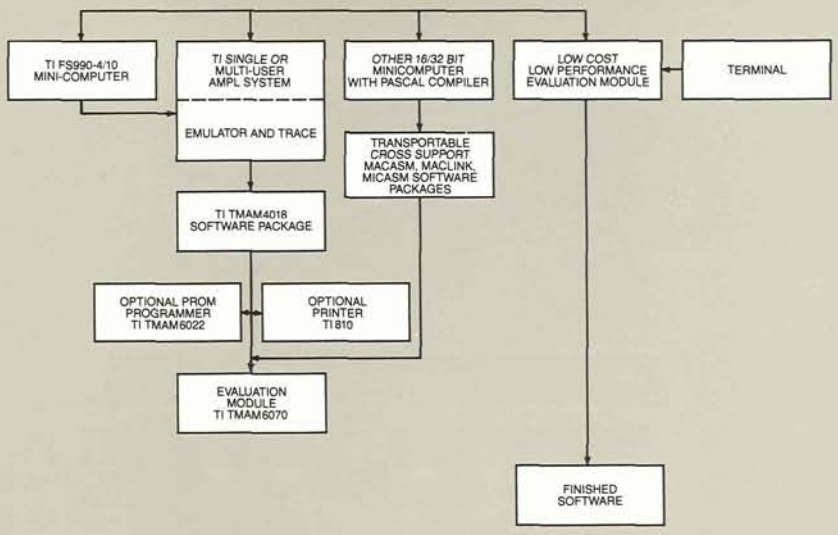
Evaluation Module (EVM)

The TMS7000 Series Evaluation Module consists of two boards plus relevant software. The first board contains all the necessary hardware/software to support stand-alone operation for in-circuit emulation. The user's unique software (up to 4,096 bytes) is executed from on-board EPROMs and the board communicates via a 40-pin ribbon cable which plugs directly into the user's target board socket.

The second EVM board has an on-board monitor to provide easy software debug capability, RS232 interface, and RAM storage. When used in conjunction with a terminal or minicomputer (via the RS232 interface) the Evaluation Module can function as a very low cost software evaluation tool for single-chip microcomputer applications.

The Evaluation Module now provides software debug and breakpoint capability. Assembly capability will also be available late 1981. The operation of the Evaluation Module is restricted to the standard TMS7000 Series instruction set.

TMS7000 SOFTWARE DEVELOPMENT OPTIONS



AMPL* Development System

AMPL* stands for "Advanced Microprocessor Prototyping Laboratory" which is a complete TI system of hardware and software tools to maximize software development productivity for all of TI's microcomputer and microprocessor device families. AMPL includes a video display terminal, hard-disk (for multiple users) or floppy diskette (for single users) mass storage, and extensive software that runs on FS990 or TMAM9000 Series minicomputers.

The following software packages are part of the TMS7000 Series AMPL development system.

- **MACASM — MACRO ASSEMBLER**
  - — General cross assembler to support TMS7000 Series standard instruction set.
  - — Used in conjunction with MICASM (see below) to support user defined nonstandard TMS7000 Series instruction sets.
- **MACLINK — LINK EDITOR**
  - — Links relocatable program modules produced by MACASM.
- **MICASM — MICRO ASSEMBLER**
  - — Only required when user wishes to modify or redefine standard TMS7000 Series instruction set.
- **AMPL UTILITY**
  - — Controls emulator and trace modes of operation.

TMAM9000 AMPL SYSTEM

The AMPL Development System can be configured with optional equipment such as printer, EPROM programmer, trace module, buffer module, and emulator memory expansion. The AMPL System provides extremely powerful editing, assembly, loading, execution, and in-circuit emulation capabilities for both standard and user defined instruction sets.

If a potential user is considering modifying the standard TMS7000 Series instruction set, a local TI Regional Technology Center can provide engineering support. TI can also provide the specific information needed for microprogramming the TMS7000 Series.

Transportable Cross Support (in Development)

The main software packages for TMS7000 Series AMPL described above (MACASM, MACLINK and MICASM in PASCAL) is expected to be available in transportable cross support versions in late 1981, allowing customers to use most 16-bit minicomputers with resident Pascal compilers.

TI Design Support

Another option available to the potential TMS7000 Series user is to contract with TI to provide all the software and hardware design resources required to realize the desired application. A local TI Regional Technology Center (RTC) will contract with TMS7000 Series customers to provide this design engineering service.

In addition, the local RTC's can provide the indepth training that could be required to fully utilize the advanced feature of the TMS7000 Series — such as microprogramming. Contact with a RTC or the main plant can be coordinated either by your local TI Field Sales Engineer or directly.

Complete TMS7000 Series documentation including data manuals, programming manuals, and microprogramming information is readily available. Call your local TI Field Sales Engineer or one of the numbers below for more information. Let us show you how the state-of-the-art TMS7000 Microcomputer Series can give you the winning price/performance edge over the competition.

For direct service, call:

Boston RTC	(617) 890-6671
Chicago RTC	(312) 640-2909
Southern California RTC	(714) 540-7311
Factory (Houston)	(713) 778-6549

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TI Sales Offices

ALABAMA: Huntsville, 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix, P.O. Box 35160, 8102 N. 23rd Ave., Suite A, Phoenix, AZ 85069, (602) 249-1313.

CALIFORNIA: El Segundo, 831 S. Douglas St., El Segundo, CA 90245, (213) 973-2571; **Irvine,** 17620 Fitch, Irvine, CA 92714, (714) 545-5210; **Sacramento,** 1900 Point West Way, Suite 171, Sacramento, CA 95815, (916) 929-1521; **San Diego,** 4333 View Ridge Ave., Suite B., San Diego, CA 92123, (714) 278-9600; **Sunnyvale,** P.O. Box 9064, 776 Palomar Ave., Sunnyvale, CA 94086, (408) 732-1840; **Woodland Hills,** 21220 Erwin St., Woodland Hills, CA 91364, (213) 704-7759.

COLORADO: Denver, 9725 E. Hampden St., Suite 301, Denver, CO 80231, (303) 695-2800.

CONNECTICUT: Wallingford, 9 Barnes Industrial Park Rd., Barnes Industrial Park, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Clearwater, 2280 U.S. Hwy. 19 N., Suite 232, Clearwater, FL 33515, (813) 325-1861; **Ft. Lauderdale,** 2765 N.W. 62nd St., Ft. Lauderdale, FL 33309, (305) 973-8502; **Winter Park,** 1850 Lee Rd., Suite 115, Winter Park, FL 32789, (305) 644-3535.

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