VL82C101B

PC/AT-COMPATIBLE SYSTEM CONTROLLER

FEATURES

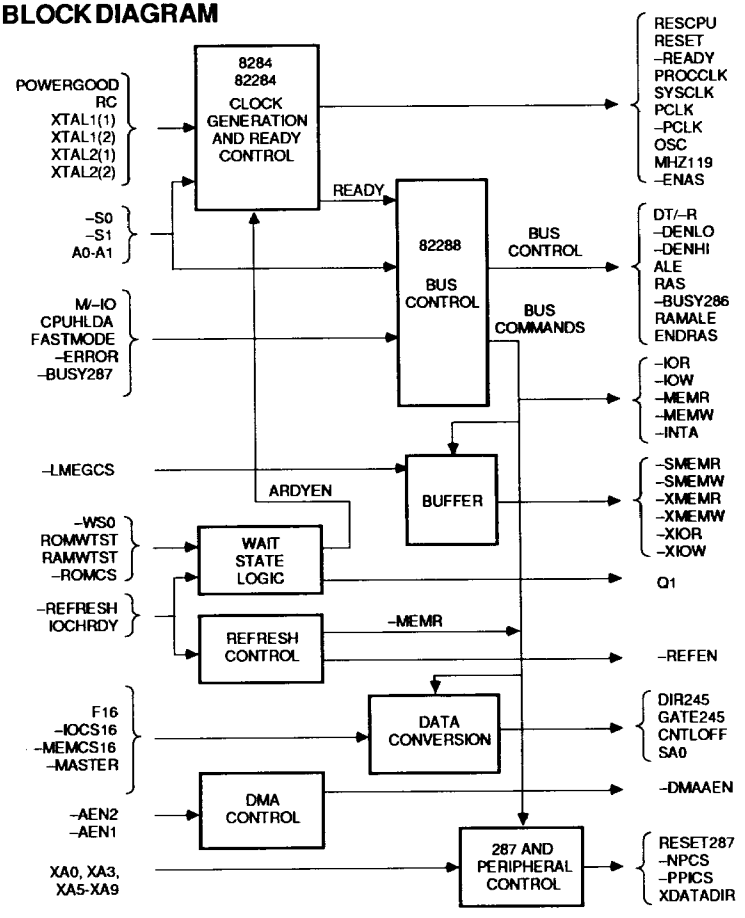
- Fully compatible with IBM PC/AT-type designs
- Replaces 36 integrated circuits on the PC/AT-type board
- Supports up to 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Sink 20 mA on slot driver outputs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C101B PC/AT-Compatible System Controller replaces an 82C284 Clock Controller and 82C288 Bus Controller (both are used in '286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately 31 other less complex integrated circuits used as Wait State logic. When used in 12 MHz systems utilizing 80 ns DRAMs, the device provides the required one wait state for a "write" operation, and zero wait states for a "read" operation. A 12 MHz system using 120 ns DRAMs will be provided with one wait state for "write" and one wait state for "read". The device accepts both the 24 MHz crystal to control the system clock as well as the 14.318 MHz crystal to control the video clock. It also supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C101B is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C101B-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

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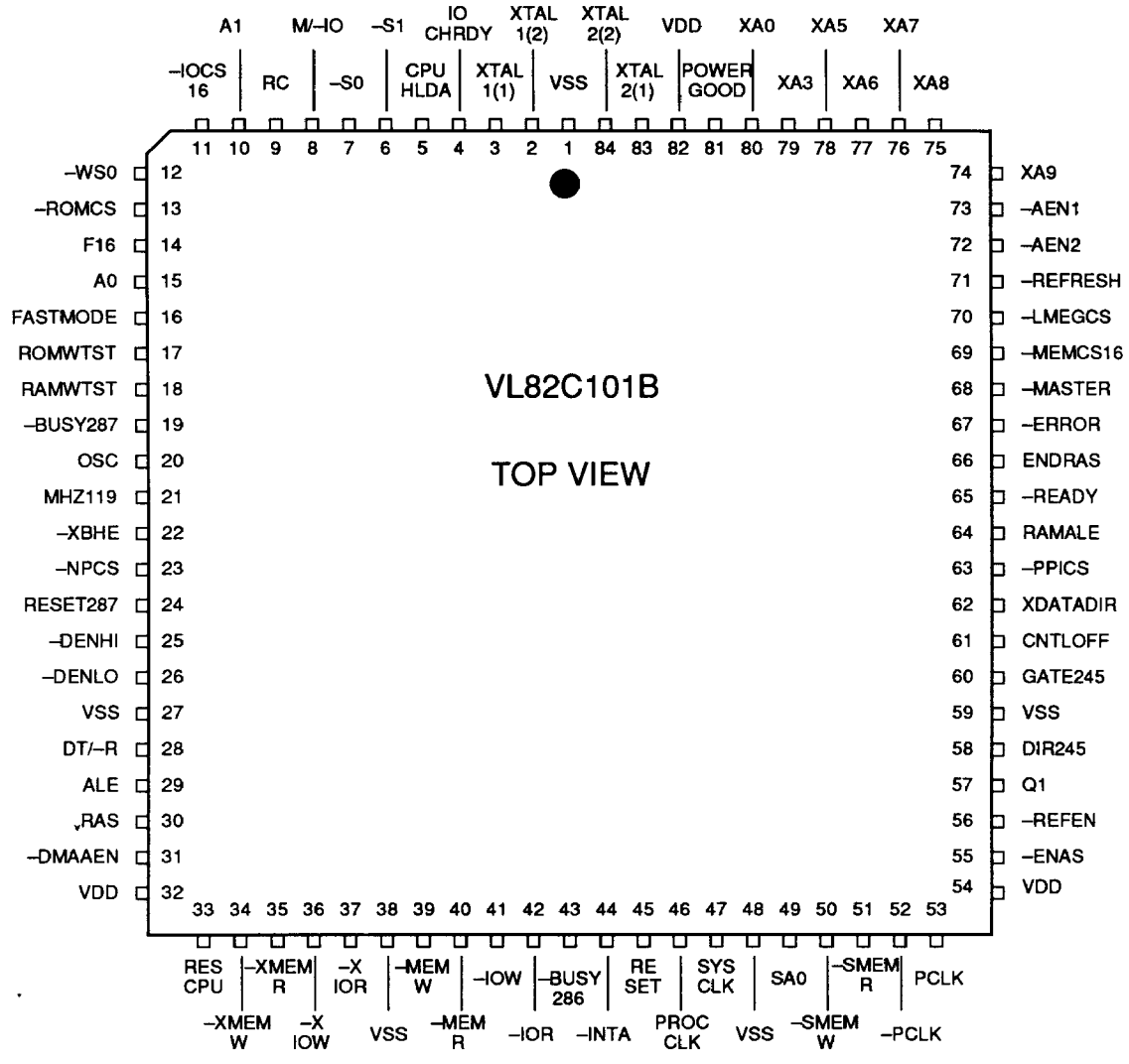
PIN DIAGRAM


A1
M/–IO
–S1
IO CHRDY
XTAL 1(2)
XTAL 2(2)
VDD
XA0
XA5
XA7
–IOCS 16
RC
–S0
CPU HLDA
XTAL 1(1)
VSS
XTAL 2(1)
POWER GOOD
XA3
XA6
XA8
11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75
–WS0 12
–ROMCS 13
F16 14
A0 15
FASTMODE 16
ROMWTST 17
RAMWTST 18
–BUSY287 19
OSC 20
MHZ119 21
–XBHE 22
–NPCS 23
RESET287 24
–DENHI 25
–DENLO 26
VSS 27
DT/–R 28
ALE 29
–RAS 30
–DMAAEN 31
VDD 32
74 XA9
73 –AEN1
72 –AEN2
71 –REFRESH
70 –LMEGCS
69 –MEMCS16
68 –MASTER
67 –ERROR
66 ENDRAS
65 –READY
64 RAMALE
63 –PPICS
62 XDATADIR
61 CNTLOFF
60 GATE245
59 VSS
58 DIR245
57 Q1
56 –REFEN
55 –ENAS
54 VDD
VL82C101B
TOP VIEW
33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
RES CPU
–XMEM W
–XMEM R
–X IOW
–X IOR
VSS
–MEM W
–MEM R
–IOW
–IOR
–BUSY 286
–INTA
RE SET
PROC CLK
SYS CLK
VSS
SA0
–SMEM W
–SMEM R
–PCLK
PCLK

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
XTAL1(2)	2	O	Crystal 1 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This is the crystal output.
XTAL1(1)	3	I	Crystal 1 Input 1 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This input drives the internal oscillator and determines the frequency of OSC.
IOCHRDY	4	I	I/O Channel Ready - This input is generated by an I/O device. When low, it indicates a not ready condition. This is used to extend memory or I/O accesses by inserting wait states. When high, this signal allows normal completion of a memory or I/O access by an I/O device.
CPUHLDA	5	I	CPU Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–S1	6	I	Status 1 - An active low input/pull-up from the CPU in combination with –S0 and M/–IO determine which type of bus cycle to initiate. –S1 going active indicates a read cycle unless –S0 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or halt/shutdown operation.
–S0	7	I	Status 0 - An active low input/pull-up from the CPU in combination with –S1 and M/–IO determine which type of bus cycle to initiate. –S0 going active indicates a write cycle unless –S1 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or a halt/shutdown operation.
M/–IO	8	I	Memory or I/O Select - This input indicates the type of bus cycle to be performed. If high, a memory cycle or halt/shutdown cycle is started. If low, then an I/O cycle or an interrupt acknowledge cycle will be initiated.
RC	9	I	This active low input signal will force a CPU reset when active. It is generated by the keyboard controller.
A1	10	I	CPU Address Bus Bit 1 - This input is used to determine when to initiate a shutdown operation. A shutdown will be started when A1 is low, M/–IO is high, and both –S0 and –S1 go low.
–IOCS16	11	I	I/O Chip Select 16 - This active low input is generated by an I/O device for a 16-bit data bus access.
–WS0	12	I	Wait State 0 - This active low input signal should have an external pull-up. A peripheral device can pull this signal low to force a zero wait state cycle.
–ROMCS	13	I	ROM Chip Select - This active low input is a signal generated from –LCS0ROM and –LCS1ROM and is used to indicate a ROM memory access.
F16	14	I	This input indicates a word memory access. It is used to inhibit command delays during a 16 bit memory access.
A0	15	I	CPU Address Bus Bit 0 - This input is used to generate enable signals for the data bus transceivers.
FASTMODE	16	I	This active high input enables the generation of an early ALE signal, called RAMALE, from the edge of –MEMR or –MEMW. If FASTMODE is desired, this pin must be held low until after the first memory read cycle. RAMALE is equal to ALE when FASTMODE is inactive.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
ROMWTST	17	I	ROM Wait State - This input is used to select the desired number of ROM access wait states. ROMWTST = 0 indicates two waits while RAMWTST = 1 indicates one wait state. If two wait state mode is required, this pin must be set high when CPUHLDA (pin 5) is high.
RAMWTST	18	I	RAM Wait State - This input is used to select the desired number of RAM access wait states. RAMWTST = 0 indicates zero waits while RAMWTST = 1 indicates one wait state.
–BUSY287	19	I	Busy 287 - A busy status input that is asserted by the 80287 to indicate that it is currently executing a command.
OSC	20	O	This is the buffered output of XTAL1 oscillator.
MHZ119	21	O	This output is the OSC output clock divided by 12. It is used by the Peripheral Controller device for the timer controller.
–XBHE	22	I/O	Transfer Byte High Enable - This active low I/O is used to allow the upper data byte of be passed through the data bus transceivers.
–NPCS	23	O	Numerical Processor Chip Select - This active low output is the chip select for the 80287 numerical processor.
RESET287	24	O	Reset 287 - This active high output is used to reset the 80287 numerical processor.
–DENHI	25	O	Data Bus Enable High - This active low output is used to enable the data bus transceiver on the high byte of the data bus.
–DENLO	26	O	Data Bus Enable Low - This active low output is used to enable the data bus latch byte accesses.
DT/–R	28	O	Data Transmit/Receive - An output that determines the data direction to and from the local data bus. A high indicates a write bus cycle and a low indicates a read bus cycle. DT/–R is high when no bus cycle is active. –DENLO and –DENHI are always inactive when DT/–R changes state.
ALE	29	O	Address Latch Enable - A positive edge output that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
RAS	30	O	This output will go active anytime a memory read or memory write command is issued.
–DMAAEN	31	O	DMA Address Enable - An active low output that is active whenever an I/O device is making a DMA access to the system memory.
RESCPU	33	O	Reset CPU - This is the active high output system reset for the CPU. It is generated from POWERGOOD, RC or when a shut down status is generated by the CPU.
–XMEMW	34	I/O	Peripheral Bus Memory Write - An active low I/O that is the memory write command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XMEMR	35	I/O	Peripheral Bus Memory Read - An active low I/O that is the memory read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XIOW	36	I/O	Peripheral Bus Input/Output Write - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–XIOR	37	I/O	Peripheral Bus Input/Output Read - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–MEMW	39	I/O	Memory Write - This active low I/O is the memory write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–MEMR	40	I/O	Memory Read - This active low I/O is the memory read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. –MEMR is also active during a refresh cycle.
–IOW	41	I/O	Input/Output Write - This is the active low I/O write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–IOR	42	I/O	Input/Output Read - This is the active low I/O read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–BUSY286	43	O	Processor 286 Extension Busy - This output goes to the –BUSY input of the 80286. If pulled low, this signal stops the 80286 program execution on all WAIT and some ESC instructions until it returns inactive (high).
–INTA	44	O	Interrupt Acknowledge - This active low output that is three-stated, is the interrupt acknowledge command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
RESET	45	O	Reset - This active high output signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
PROCCLK	46	O	Processor Clock - This output is the processor clock for the CPU and coprocessor. It is equal to the crystal frequency on crystal oscillator input XTAL2.
SYSCLK	47	O	System Clock - This output is the main system clock. It is equal to half the PROCCLK frequency and is synchronized to the processor's T-states.
SA0	49	O	System Address Bus Bit 0 - A three-stated output.
–SMEMW	50	O	Memory Write - An active low three-stated output that is the memory write command to the expansion bus. Drives when –LMEGCS is low.
–SMEMR	51	O	Memory Read - An active low three-stated output that is the memory read command to the expansion bus.
–PCLK	52	O	Peripheral Clock Complement Phase - This output is the complement phase of the peripheral clock. It is equal to half the PROCCLK frequency and is used for clocking peripheral devices.
PCLK	53	O	Peripheral Clock True Phase - This output is the true phase of the peripheral clock. It is equal to half the PROCCLK frequency and is used for clocking peripheral devices.
–ENAS	55	O	Enable Address Strobe - This active low output is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
–REFEN	56	O	Refresh Enable - An active low output. It will be asserted when a refresh cycle is needed for the DRAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
Q1	57	O	This active high output will go active during the second phase of a CPU bus cycle following the T-state. It is used by other devices to generate the address strobe for the real time clock.
DIR245	58	O	Direction 245 - This output determines the direction of the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
GATE245	60	O	Gate 245 - This output enables the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
CNTLOFF	61	O	Control Off - This output is used to enable the lower byte data bus latch during byte accesses.
XDATADIR	62	O	Transfer Data Direction - This output controls the direction of data flow through the transceiver between the X data bus and the lower byte of the S data bus. A high indicates data flow from the S bus to the X bus. A low indicates data flow from the X bus to the S bus.
–PPICS	63	O	Programmable Peripheral Interface Chip Select - This active low output is used to generate the chip select for the keyboard controller.
RAMALE	64	O	RAM Address Latch Enable - This output is used in the FASTMODE of operation. When FASTMODE is inactive RAMALE is equal to ALE.
–READY	65	O	Ready - When active, indicates that the current bus cycle is to be completed. –READY is an open drain output requiring an external pull-up resistor.
ENDRAS	66	O	An output that is used to complete a memory read/write cycle.
–ERROR	67	I	Error - An error status input from the 80287. This reflects the ES bit of the 80287 status word and indicates that an unmashed error condition exists.
–MASTER	68	I	Master - This active low input is asserted low by devices on the expansion bus. A low indicates that another device is active.
–MEMCS16	69	I	Memory Chip Select 16 - A low on this pin indicates that the off-board memory is 16-bits wide.
–LMEGCS	70	I	Lower Megabyte Chip Select - This input indicates that the lower memory address space (0-1 megabyte) is selected. When low, it enables the three-state drivers on –SMEMR and –SMEMW.
–REFRESH	71	I	Refresh - This active low input is used to initiate a refresh cycle for the dynamic RAMs.
–AEN2	72	I	Address Enable 2 - This active low input is from the DMA controllers and is used to enable the address latches for 16 bit data transfers.
–AEN1	73	I	Address Enable 1- This active low input is from the DMA controllers and is used to enable the address latches for 8 bit data transfers.
XA5-XA9	78-74	I	Peripheral Address Bus Bits 5-9 - These inputs are used to decode chip select and reset signals for the coprocessor.
XA3	79	I	Peripheral Address Bus Bit 3 - This input is used in control of the coprocessor reset and chip select signals.
XA0	80	I	Peripheral Address bus bit 0 - This input is used in control of the coprocessor and 8/16-bit data conversions.
POWERGOOD	81	I	System Power-on Reset - This input signal indicates that power to the board is stable. A Schmitt-trigger input is used so the input can be connected directly to an RC network.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
XTAL2(1)	83	I	Crystal 2 Input 1- A parallel resonant fundamental mode crystal should be attached across XTAL2(1) and XTAL2(2). This input drives the internal oscillator and determines the frequency for PROCCLK.
XTAL2(2)	84	O	Crystal 2 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL2(1) and XTAL2(2). This is the crystal output.
VDD	32, 54, 82		System Power: 5 V
VSS	1, 27, 38, 48, 59		System Ground

FUNCTIONAL DESCRIPTION

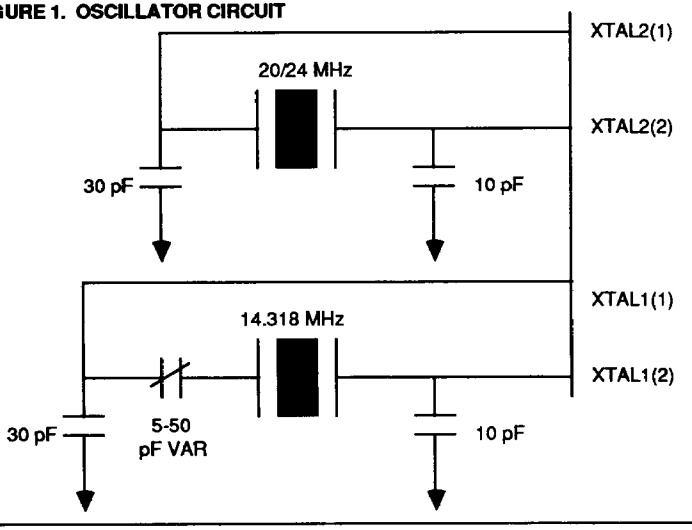
The VL82C101B chip generates all the major clocks for an AT-compatible system design along with the command and control signals for both the system and peripheral buses. It interfaces with the CPU to determine the type of bus cycle to execute and generates the –READY signal to indicate that the current bus cycle can be terminated. It also contains logic to make conversions between 16 bit and 8 bit data accesses. Finally, it generates some of the control signals necessary for the 80287 Numerical Processor.

CLOCK GENERATION

The VL82C101B contains two oscillators to generate the clocks for an AT-compatible design. Both oscillators are designed to use an external, parallel resonant fundamental mode crystal. The first oscillator is used to generate the video clock output (OSC) and MHZ119 which is the clock for the 8254 timer in the Peripheral Controller device. A 14.318 MHz crystal should be used on this oscillator to maintain compatibility. The OSC output is generated directly from this oscillator for the system bus and the MHZ119 output is derived from the OSC output divided by 12. To guarantee sufficient drive and a clean signal on the slots it is recommended that the OSC output be buffered before driving the expansion connectors.

The second oscillator is used to generate the system clocks. The crystal frequency for this oscillator should be twice the operating frequency of the CPU. For a 12 MHz system, a 24 MHz oscillator should be used. This oscillator is used to generate four clock outputs. PROCCLK is generated directly from the oscillator and will have the same frequency as the crystal input. This output is connected directly to the CPU and Numerical Processors clock inputs. PCLK and –PCLK are used to clock the keyboard controller. These outputs are free running clock signals with a frequency of half the PROCCLK frequency. The last clock output is SYSCLK. This clock is also at half the PROCCLK frequency, but it will be held low during RESET and will not begin running until the first bus cycle is initiated by the CPU. It will then make its first low to high transition on the falling edge of PROCCLK during the start of the first TC cycle (see timing waveforms). This synchronization is done to ensure that the system clock is synchronized with the 80286 internal system clock. The SYSCLK output is used to drive the Peripheral Controller device directly and should be buffered externally before driving the expansion connectors to guarantee sufficient drive and a clean signal on the slots.

FIGURE 1. OSCILLATOR CIRCUIT



RESET AND READY CONTROL

The 82284 megacell along with some support logic is used to control the system reset signals and –READY signal for the CPU. Two basic reset signals are generated for the system. RESET is the system reset out of the 82284 megacell and is synchronized to

PROCCLK. It is generated from the POWERGOOD input signal. RESCPU, the other reset output, is connected to the input on the 80286 processor. RESCPU will be active anytime RESET is active. It can also be generated from two other possible sources. The first is the RC input from the keyboard controller. RESCPU will go active within 4 to 18 PROCCLK cycles after RC is asserted and will go inactive 16 PROCCLK cycles later or 16 PROCCLK cycles after RC is negated. RESCPU will also be generated if a shutdown command cycle is decoded from the CPU. As with the RC input, RESPCU will go active within 4 to 18 PROCCLK cycles of detecting the shutdown command and will be negated 16 PROCCLK cycles later. The POWERGOOD pin has a Schmitt-trigger input so that an RC network can be used to generate the reset signals.

The –READY output is synchronized and controlled by the 82284 megacell. –READY is an open drain output connected directly to the CPU and requires an external pull-up resistor. A resistor value of 700 Ω is recommended for 10 or 12 MHz operation. Bus cycle length is controlled by the –READY output. Bus cycles are lengthened and shortened internally by the VL82C101B depending on the type of bus cycle being executed. The length of a bus cycle can be shortened externally by pulling the –WS0 input low or lengthened by pulling the IOCHRDY input low. If IOCHRDY is pulled low the bus cycle will not be terminated until IOCHRDY is returned high.

COMMAND AND BUS CONTROL

The VL82C101B contains an 82288 bus controller megacell to generate all the bus command and control signals. The 82288 megacell generates the –MEMR, –MEMW, –IOR and –IOW command signals and the DT/–R control signal. The DEN output from the megacell is split into –DENLO and –DENHI for enables on the upper and lower bytes of the data bus. Internal circuitry is used to insert one PROCCLK cycle of command delay for all I/O cycles and off-board 8 bit memory cycles. Refer to the 82288 data sheet for complete operation of the 82288 megacell.

OPERATING MODES

The VL82C101B operates in four basic modes. First, and most common, is the CPU mode. This mode is active any time the input CPUHLDA is low. While in CPU mode the VL82C101B will drive both the CMD (–MEMR, –MEMW, –IOR, –IOW) bus and XCMD (–XMEMR, –XMEMW, –XIOR, –XIOW) bus.

The other modes can only be active when CPUHLDA is high. Then the VL82C101B can be in DMA mode, –MASTER mode, or –REFRESH mode. If the inputs –AEN1 or –AEN2 are active, the VL82C101B is in DMA mode and the CMD bus is driven from the inputs on the XCMD bus. If the –MASTER input is active, the VL82C101B is in –MASTER mode and the XCMD bus is driven from the inputs on the CMD bus. When the –REFRESH mode is active the –MEMR output will be driven to generate the refresh for the DRAMs but –MEMW, –IOR and –IOW will be in a high impedance state. The XCMD pins will be configured as outputs driving whatever value is on the CMD pins.

SYSTEM BOARD MEMORY CONTROL

Memory control on the system board is accomplished with three signals, RAMALE, RAS, and ENDRAS.

The system board memory controls can operate in two different modes. While in CPU mode with the FASTMODE input set low or in non-CPU mode, RAMALE will look the same as ALE and RAS will be generated from –MEMR and –MEMW. In this mode the memory timing will look the same as an AT-compatible design. If the FASTMODE input is set high, the RAMALE and RAS signals are changed during CPU mode accesses to allow for more DRAM access time.

RAMALE is used by both the Memory Controller and Address Buffer devices to latch in current address values to generate both address and enable signals for the DRAMs. In FASTMODE the RAMALE signal is changed so that it will only go low when a memory read or write command is active. This guarantees that the memory address and chip select signals will remain valid during the entire memory cycle and allows RAMALE to return high as soon as possible to transmit through the new address for the next cycle.

The RAS output is changed in FASTMODE so that it will go active one PROCCLK cycle sooner during a memory read cycle to allow more read access time. The RAS output will look the same as non-FASTMODE timing for write cycles. This was done to allow for zero wait state cycles on memory reads. RAS could not be moved up on memory writes because the data from the CPU would not be valid in time to be written into the DRAMs.

ENDRAS is used to terminate the RAS signals to the DRAMs without terminating the memory access. This allows for the required RAS precharge time before the next memory access. It will normally be high and make a high to low transition to terminate the RAS signals to the DRAMs on the third PROCCLK after RAS goes active. ENDRAS will then remain low until RAS returns low, which will cause ENDRAS to return high. The exception to this timing is for a zero wait state RAM read. In this case, ENDRAS will make the high to low transition two PROCCLK cycles after RAS instead of three.

WAIT STATE LOGIC

Wait states can be controlled from a number of different sources within the VL82C101B. It is internally programmed to generate the wait states shown in Table 1 based on the appropriate input signals.

Any of these programmed values can be overridden by the inputs IOCHRDY and –WS0. IOCHRDY can be used to extend any bus cycle. When IOCHRDY is pulled low the current bus cycle will be maintained until it is returned high. A low on –WS0 will terminate the current bus cycle as soon as it is recognized by the VL82C101B. These inputs need only be pulled low to modify the values shown in Table 1. IOCHRDY and –WS0 are mutually exclusive and only one of them should

be pulled low within a given bus cycle. Refer to the timing diagrams for setup and hold requirements.

REFRESH CONTROL

The VL82C101B contains circuitry to control a refresh cycle in an AT-compatible design. When the input –REFRESH is pulled low the VL82C101B will issue –REFEN to clock the refresh counter and enable the refresh addresses onto the memory address bus. It will also issue a –MEMR command. For correct operation –REFRESH should not be pulled low unless CPUHLDA is active.

DATA CONVERSION

A state machine for controlling the conversion between 16 bit data accesses from the CPU and 8 bit peripherals is contained in the VL82C101B. This state machine will generate the control signals DIR245, GATE245, and CNTLOFF to the Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low data byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to a high, and then perform the read/write operation for the high data byte. The VL82C101B also uses the DIR245 and GATE245 during 8-bit DMA cycles to route the lower byte on the system data bus to or from the high or low byte of on-board memory.

NUMERICAL PROCESSOR AND PERIPHERAL CONTROL

The VL82C101B generates a RESET signal and chip select signal for the 80287 Numerical Processor. The signal RESET287 is used to reset the 80287 and can be activated by a system reset or an I/O write to address 0F1 hex. –NPCS is used as a chip select for the 80287 and is decoded at addresses 0F8-0FF hex.

The VL82C101B also controls the –BUSY286 signal sent to the 80286 from the Numerical Processor. The 80287 will assert –BUSY287 whenever it is performing a task. This signal is passed to the 80286 by asserting the –BUSY286 output. Normally –BUSY286 will follow –BUSY287. However, if the –ERROR signal is asserted while the –BUSY287 signal is active, the –BUSY286 output will be latched low and will remain active until cleared by an I/O write cycle to address 0F0 hex or 0F1 hex.

TABLE 1. WAIT STATES

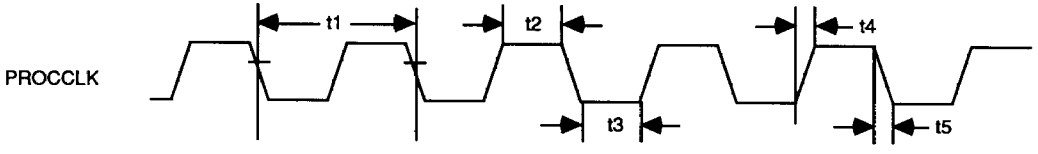
Access Type	RAMWTST	ROMWTST	F16	–MEMCS16	–IOCS16	Number of Waits
INTA Cycles	X	X	X	X	X	4
8 Bit I/O	X	X	X	X	1	4
16 Bit I/O	X	X	X	X	0	1
Off-board 8-Bit Memory	X	X	0	1	X	4
Off-board 16-Bit Memory	X	X	0	0	X	1
On-board ROM Read	X	1	1	X	X	1
On-board ROM Read	X	0	1	X	X	2
On-board RAM Write	X	X	1	X	X	1
On-board RAM Read	1	X	1	X	X	1
On-board RAM Read	0	X	1	X	X	0

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

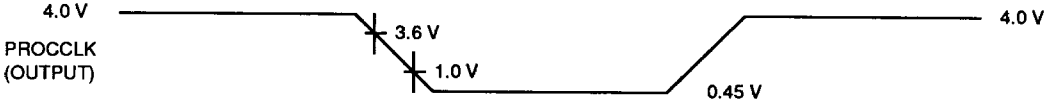
PROCCLK MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t1	PROCCLK Period	42	250	ns	24 MHz Crystal Oscillator
t2	PROCCLK High Time	14	239	ns	
t3	PROCCLK Low Time	12	237	ns	
t4	PROCCLK Rise Time		8	ns	1.0 V to 3.6 V, CL = 150 pF
t5	PROCCLK Fall Time		8	ns	3.6 V to 1.0 V, CL = 150 pF

PROCCLK TIMING WAVEFORMS



AC measurement characteristics from PROCCLK going low:



The PROCCLK (from '284 Megacell) is the main reference point for most of the AC signals. PROCCLK has a guaranteed VOH of 4.0 V and a VOL of 0.45 V. However, all AC measurements referenced to PROCCLK going low are from the 1.0 V point. At 24 MHz the transition time from 3.6 V to 1.0 V (and 1.0 V to 3.6 V) is guaranteed to be 8 ns or less.

CPU MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tSU6	POWERGOOD to PROCCLK Setup Time	20		ns	Note 1
tH7	POWERGOOD from PROCCLK Hold Time	10		ns	Note 1
tD8	RESET from PROCCLK Delay		25	ns	
tD9	SYSCLK, PCLK, –PCLK from PROCCLK Delay		25	ns	
tD10	RESCPU from PROCCLK Delay		24	ns	
tSU11	M/–IO, A1 to –S0, –S1 Setup Time	22		ns	
t12	OSC Rise/Fall Time		8	ns	CL = 100 pF
t13	MHZ119 Rise/Fall Time		8	ns	CL = 100 pF
tD14	MHZ119 from OSC Delay		20	ns	
tSU15	–S0, –S1 to PROCCLK Setup Time	24		ns	
tH16	–S0, –S1 from PROCCLK Hold Time	3		ns	
tD17	ALE Valid from PROCCLK Delay		19	ns	
tD18	DT/–R Low from PROCCLK Delay		28	ns	
tD19	DT/–R High from PROCCLK Delay		45	ns	
tD20	DT/–R High from –DENHI, –DENLO High Delay	3		ns	
tD21	–DENLO, –DENHI Active from PROCCLK Delay		35	ns	
tD22	–DENLO, –DENHI Inactive from PROCCLK Delay		35	ns	
tD23	–READY Active from PROCCLK Delay		20	ns	
tD24	–READY Inactive from PROCCLK Delay	3		ns	Note 2
tD25	–IOR, –XIOR Valid from PROCCLK Delay		40	ns	
tD26	–IOW, –XIOW Valid from PROCCLK Delay		40	ns	
tD27	XDATADIR Valid from PROCCLK Delay		40	ns	
tSU28	–IOCS16 PROCCLK Setup Time	30		ns	
tH29	–IOCS16 PROCCLK Hold Time	10		ns	
tSU30	IOCHRDY to PROCCLK Setup Time	25		ns	
tD31	–ENAS Valid from PROCCLK Delay		30	ns	
tD32	RAMALE Valid from PROCCLK Delay		24	ns	

Notes: 1. POWERGOOD is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific PROCCLK edge.

2. –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. We recommend 700 Ω for the pull-up resistor for 10 MHz and 12 MHz systems.

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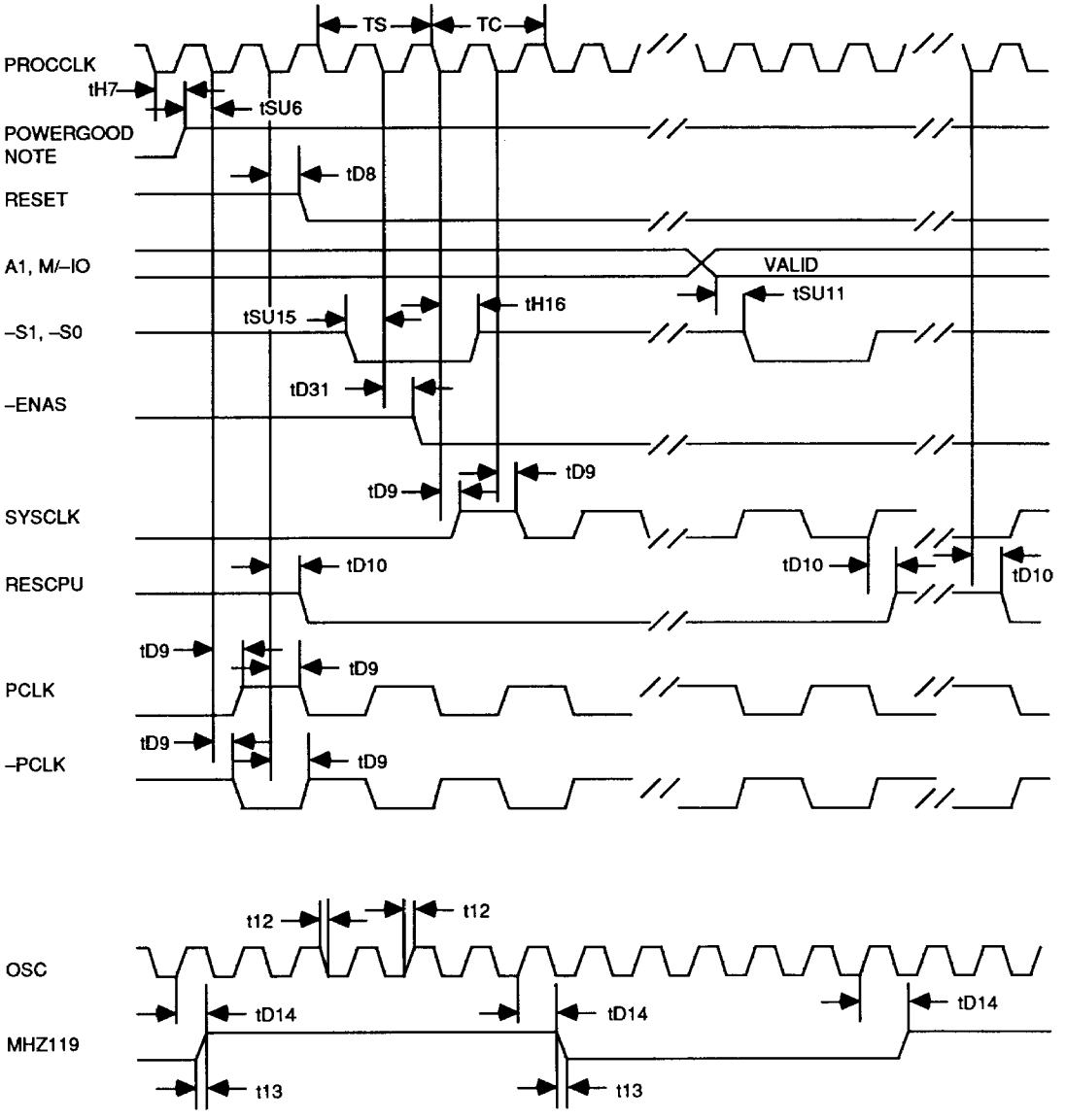
CPU MODE TIMING (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
tD33	RAS High from PROCCLK Delay		18	ns	Note 3
tD34	RAS High from PROCCLK Delay		15	ns	FASTMODE = 1, MEM Read Only
tD35	RAS Low from PROCCLK Delay		28	ns	
tD36	ENDRAS Low from PROCCLK Delay		25	ns	
tD37	ENDRAS High from PROCCLK Low Delay		55	ns	
tD38	ENDRAS High from RAS Low Delay	3		ns	
tD39	–MEMR, –XMEMR, –SMEMR Valid from PROCCLK Delay		40	ns	
tD40	–MEMW, –XMEMW, –SMEMW Valid from PROCCLK Delay		40	ns	
tSU41	–WS0 to PROCCLK Setup Time	22		ns	
tH42	–WS0 from PROCCLK Hold Time	1		ns	
tSU43	F16 to PROCCLK Setup Time	30		ns	
tH44	F16 from PROCCLK Hold Time	10		ns	
tSU45	–MEMCS16 to PROCCLK Setup Time	32		ns	
tH46	–MEMCS16 from PROCCLK Hold Time	5		ns	
tSU47	A0 to PROCCLK Setup Time	38		ns	
tD48	SA0 from PROCCLK Delay Time		35	ns	
tSU49	–XBHE to PROCCLK Setup Time	30		ns	
tD50	Q1 from PROCCLK Delay Time		35	ns	
tD51	CNTLOFF from PROCCLK Delay Time		25	ns	Note 4
tD52	DIR245 from PROCCLK Delay Time		45	ns	
tD53	GATE245 from PROCCLK Delay Time		55	ns	
tD54	–INTA Valid from PROCCLK Delay Time		42	ns	

Notes: 3. FASTMODE = 1, MEM write only. FASTMODE = 0, MEM read only.

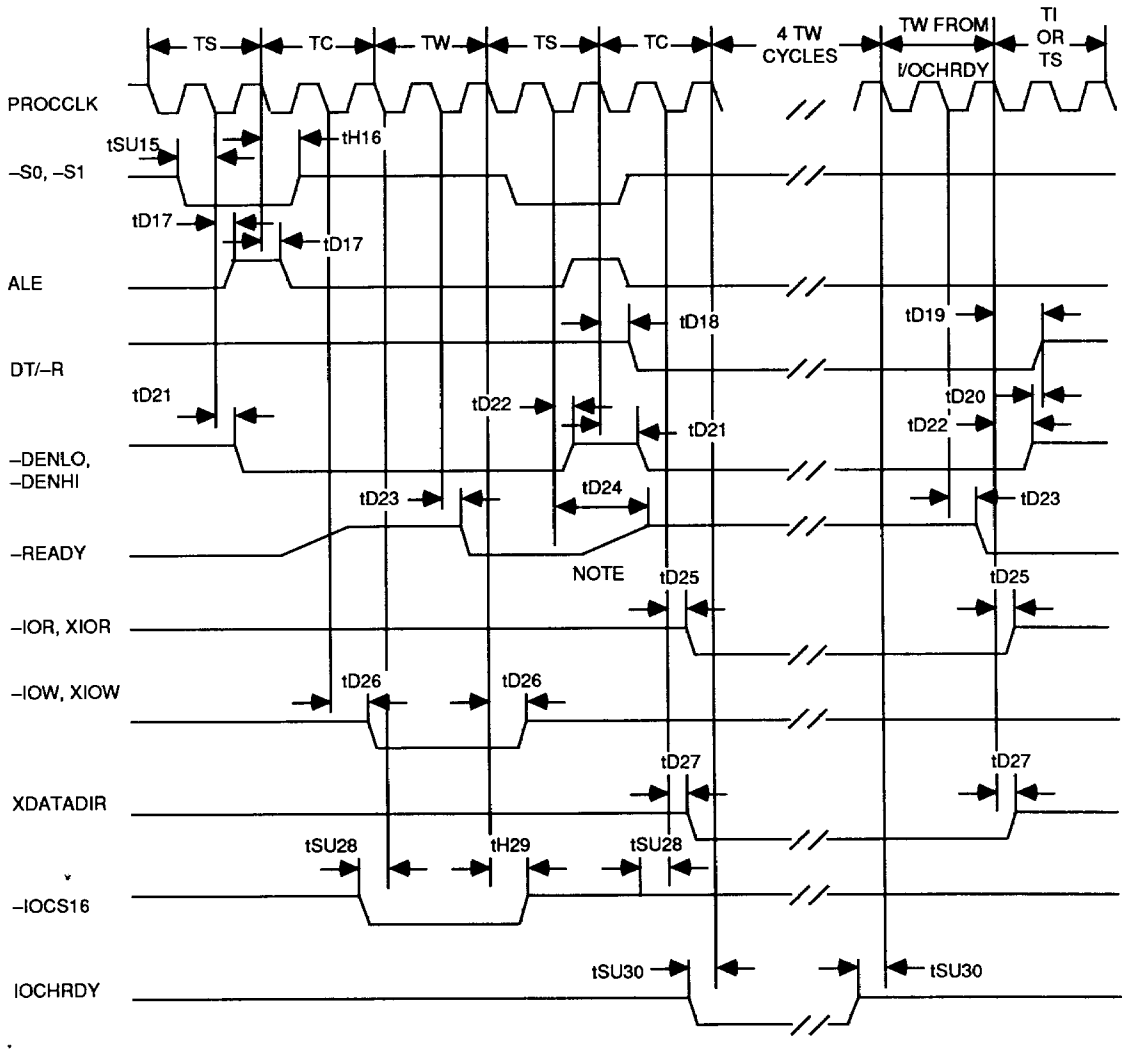
4. DIR245 goes low for a write cycle. It will remain high for read cycles.

RESET AND CLOCK TIMING WAVEFORMS



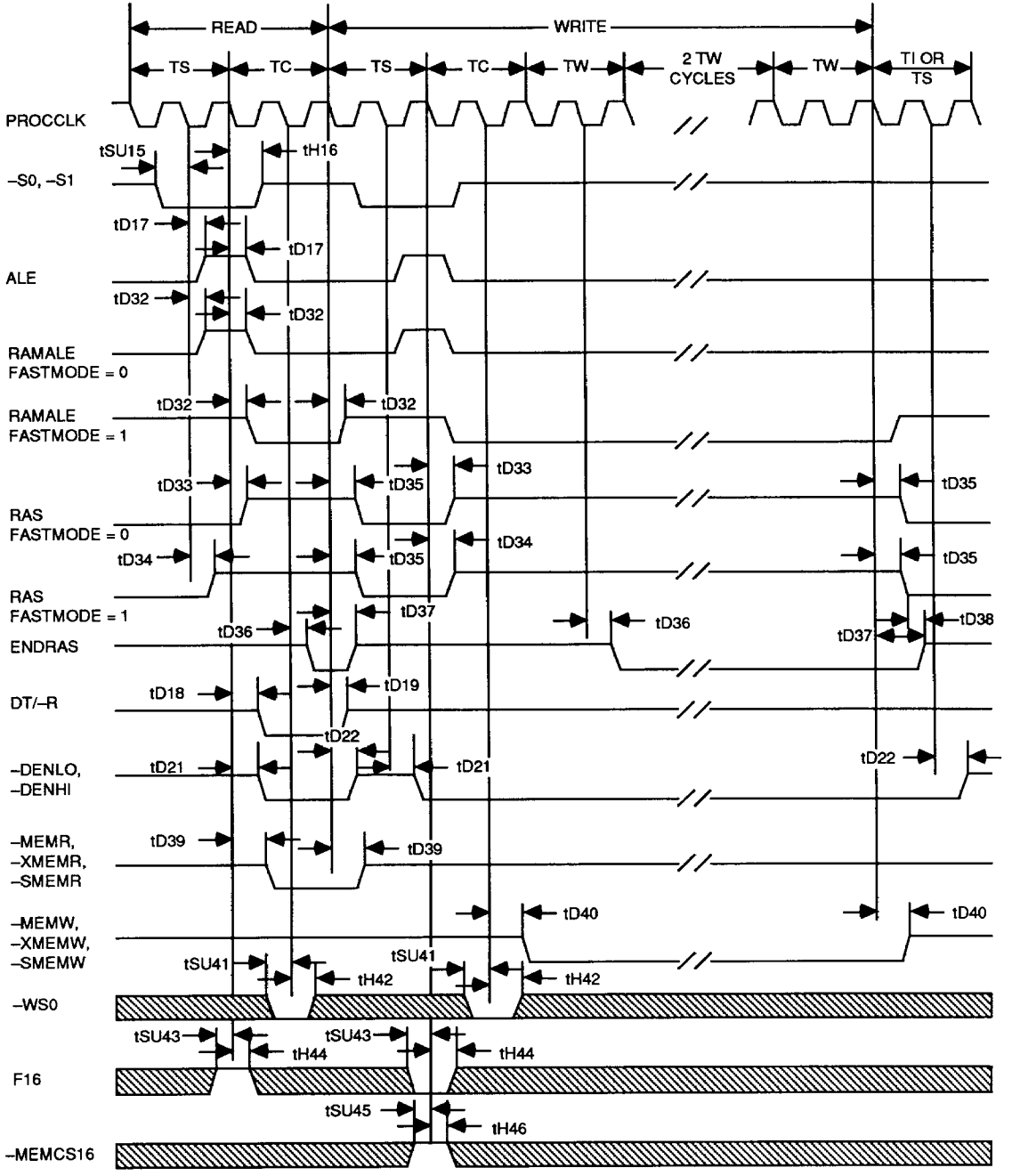
Note: POWERGOOD is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific PROCCLK edge.

I/O TIMING WAVEFORM

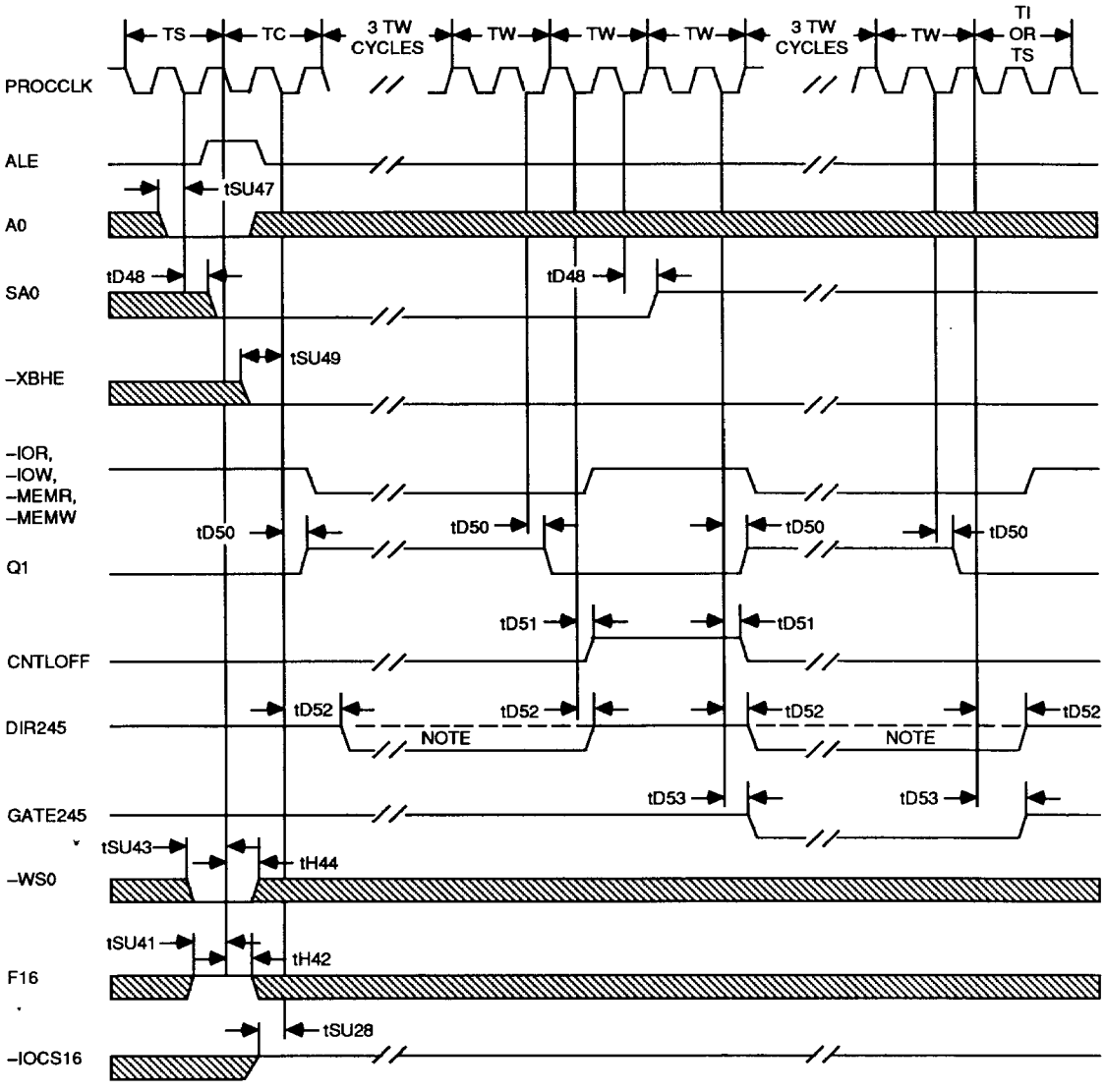


Note: –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. We recommend 700 Ω for the pull-up resistor for 10 MHz and 12 MHz systems.

MEMORY TIMING WAVEFORM

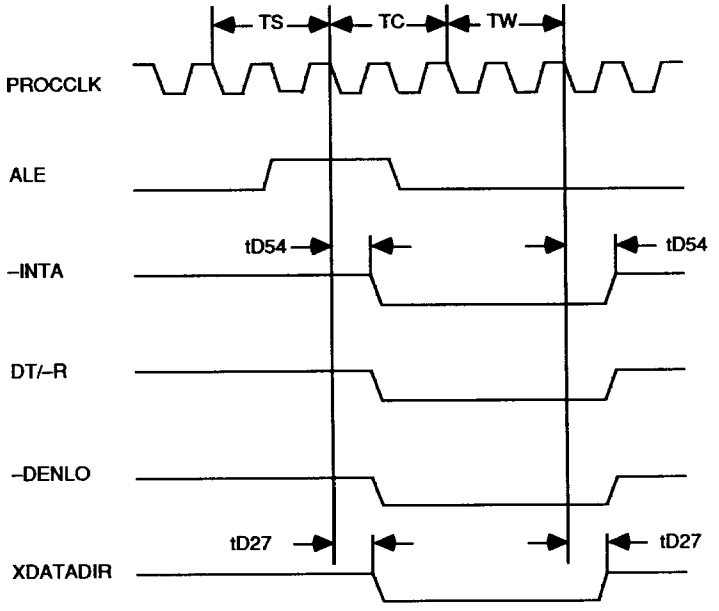


CONVERSION TIMING WAVEFORM



Note: DIR245 goes low for a write cycle. It will remain high for read cycles.

INTA TIMING WAVEFORM

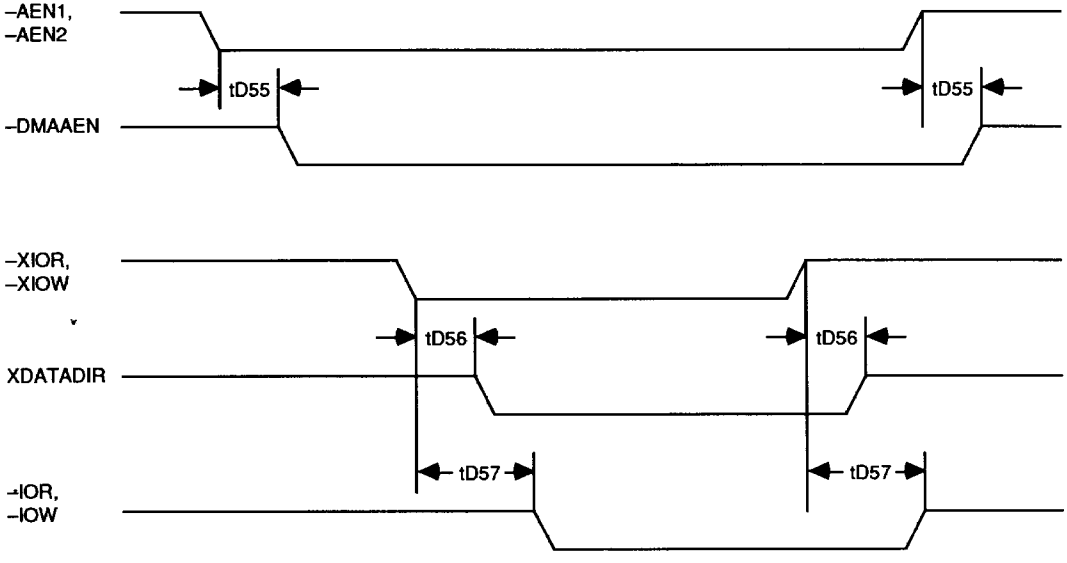


DMA MODE TIMING

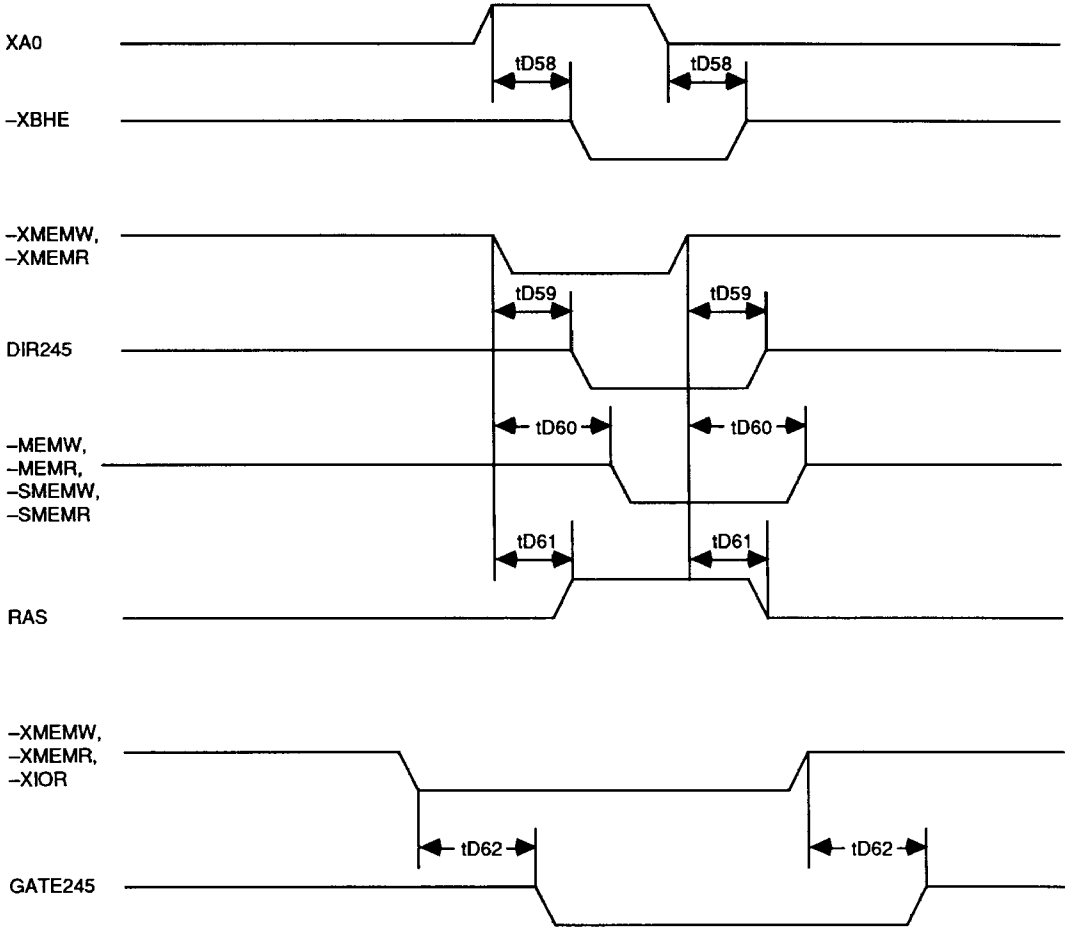
Symbol	Parameter	Min	Max	Unit	Condition
tD55	–DMAAEN Delay		20	ns	Note 1
tD56	XDATADIR Delay		27	ns	From –XIOR
tD57	–IOR, –IOW Delay		40	ns	
tD58	–XBHE Delay		35	ns	Note 2
tD59	DIR245 Delay		35	ns	
tD60	–MEMW, –MEMR, –SMEMW, –SMEMR Delay		40	ns	
tD61	RAS Delay		35	ns	
tD62	GATE245 Delay		40	ns	–AEN1 Only

Notes: 1. Either –AEN1 or –AEN2 forces –DMAAEN low.
2. During –AEN2, –XBHE is low; during –AEN1, –XHBE follows XA0 inverted.

DMA MODE TIMING WAVEFORMS



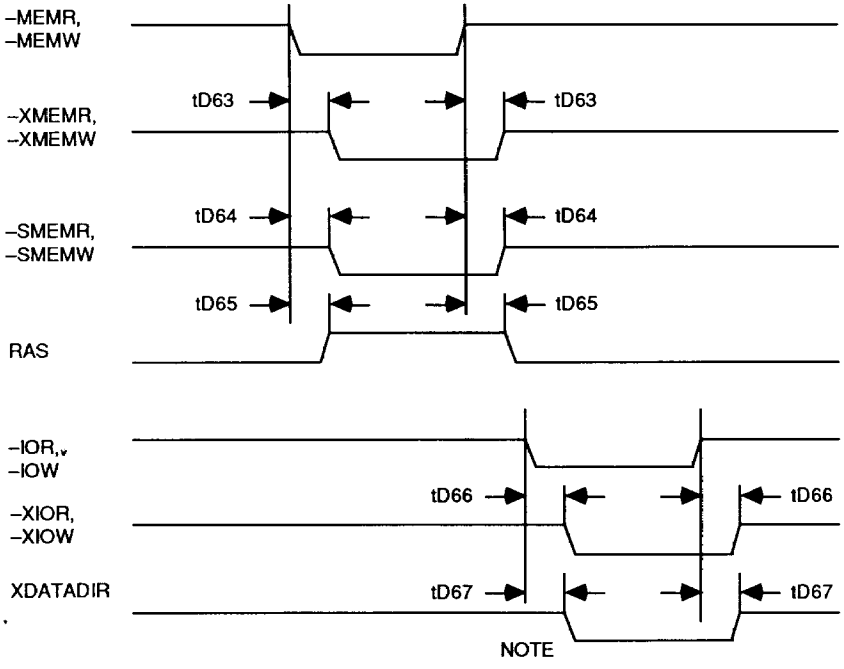
DMA MODE TIMING WAVEFORMS (Cont.)



BUS MASTER MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD63	–XMEMR, –XMEMW from –MEMR, –MEMW Delay		250	ns	
tD64	–SMEMR, –SMEMW from –MEMR, –MEMW Delay		239	ns	
tD65	RAS from –MEMR, –MEMW Delay		237	ns	
tD66	–XIOR, –XIOW from –IOR, –IOW Delay		8	ns	
tD67	XDATADIR from –IOR, –IOW Delay		8	ns	

BUS MASTER MODE TIMING WAVEFORM

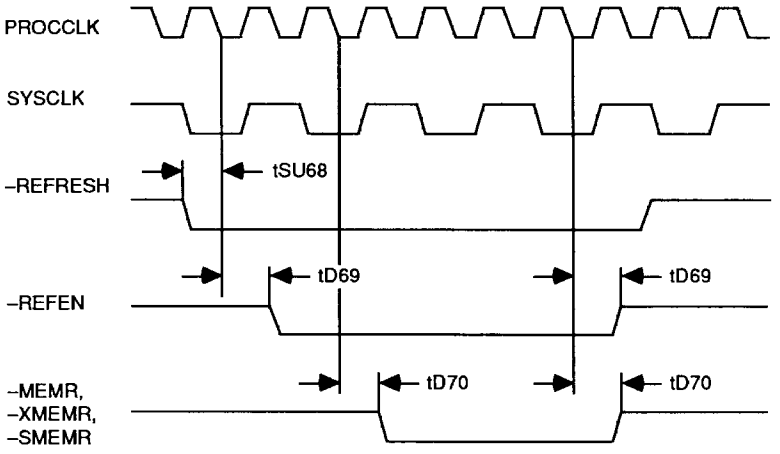


Note: XDATADIR goes low only for –IOR when XA9, XA8 are low and –NPCS is not active.

REFRESH TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tSU68	–REFRESH to PROCCLK Setup Time	20		ns	
tD69	–REFEN from PROCCLK Delay Time		35	ns	
tD70	–MEMR, –XMEMR, –SMEMR from PROCCLK Delay Time		60	ns	

REFRESH TIMING WAVEFORM



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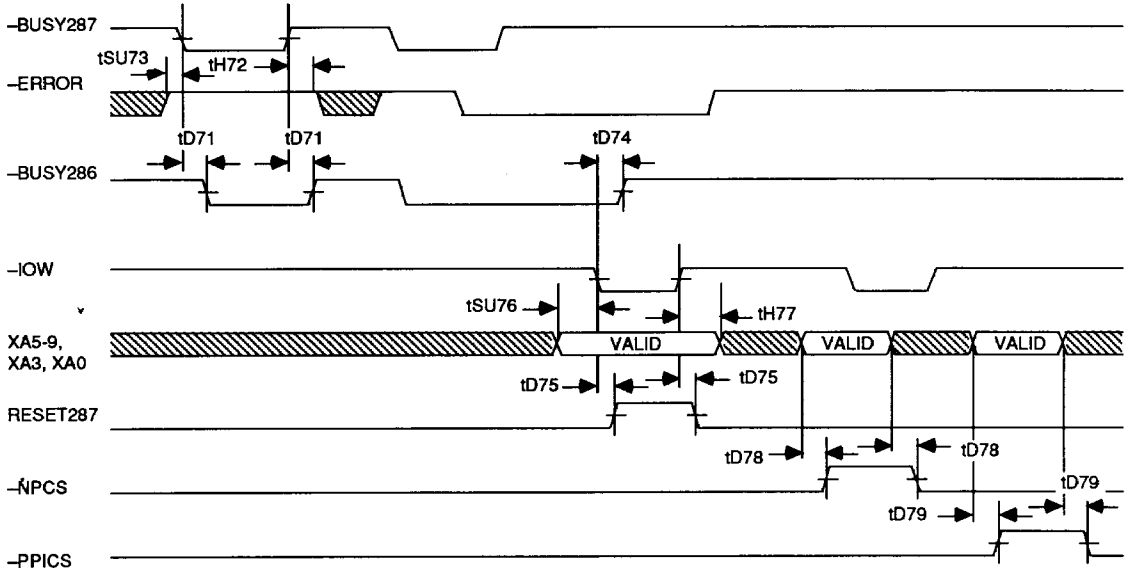
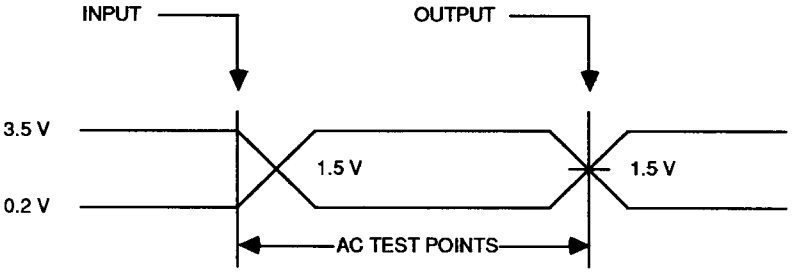
NUMERICAL PROCESSOR INTERFACE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD71	–BUSY286 from –BUSY287 Delay		35	ns	
tH72	–ERROR from –BUSY287 Hold Time	15		ns	
tSU73	–ERROR to –BUSY287 Setup Time	20		ns	
tD74	–BUSY286 from –IOW Delay		35	ns	
tD75	RESET287 from –IOW Delay		35	ns	
tSU76	XA Inputs to –IOW Setup Time	25		ns	
tH77	XA Inputs from –IOW Hold Time	20		ns	
tD78	XA Inputs to –NPCS Delay		35	ns	
tD79	XA Inputs to –PPICS Delay		35	ns	

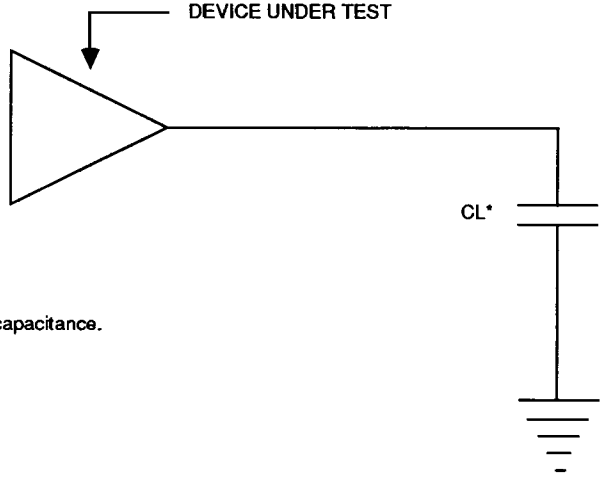
NUMERICAL PROCESSOR INTERFACE TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
49	200
39-42, 46, 50, 51, 65	150
20-22, 31, 34-37, 45, 47,	100
29	60
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to + 7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 20 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOL3	Output Low Voltage		0.45		IOL = 2 mA, All Other Pins
VIH	Input High Voltage	2.0	VDD + 0.5	V	Except POWERGOOD
VIL	Input Low Voltage	–0.5	0.8	V	
VIHS	Input High Voltage	4.0	VDD + 0.5	V	POWERGOOD, Schmitt-trigger
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	Except –S0, –S1, XTAL1(2), XTAL2(2)
ILIS	Input Leakage Current	–0.5	0.01	µA	–S0, –S1, Note 3
ILIX	Input Leakage Current	50	50	µA	XTAL1(2), XTAL2(2)
ICC	Power Supply Current		20	mA	Note 4

Notes: 1. Pins 39-42 and 49-51.
2. Pins 20-22, 31, 34-37, 45-47 and 65.
3. –S1 and –S0 have small pull-up resistors to VDD and source up to 0.5 mA when pulled low.
4. Inputs = VSS or VDD, outputs not loaded.