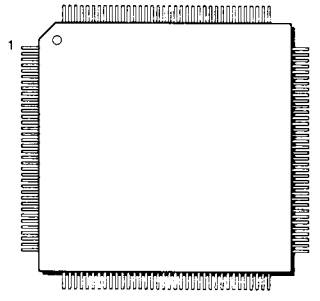
SIERRA SEMICONDUCTOR

SC18000/SC18005
Multimedia System Controller

FEATURES

- ☐ AdLib™ Register Emulation
- ☐ Sound Blaster™ 8-bit Record and Playback Compatible
- ☐ Subset of Roland MPU-401™ MIDI Commands
- ☐ Aria™ Sampled Instrument Synthesizer
- ☐ ISA Bus 16-bit DMA Transfers
- ☐ Serial 16-bit DAC/ADC Interface and DMA Logic
- ☐ Extended RAM/ROM Interface Address Space up to 32 Megabytes
- ☐ Zero Wait State Interface
- ☐ System Clock Generation

144-PIN QUAD FLAT PACKAGE



SC18000CQ
SC18005CQ

GENERAL DESCRIPTION

The SC18000 and the SC18005 make up the core of Sierra's Audio chip sets. The SC18000/5 is responsible for the interface to the PC and is designed to be compatible with the 16 bit Industry Standard Architecture (ISA) bus. The chips are in a 5 volt CMOS process and are packaged in a 144 pin plastic quad flat pack.

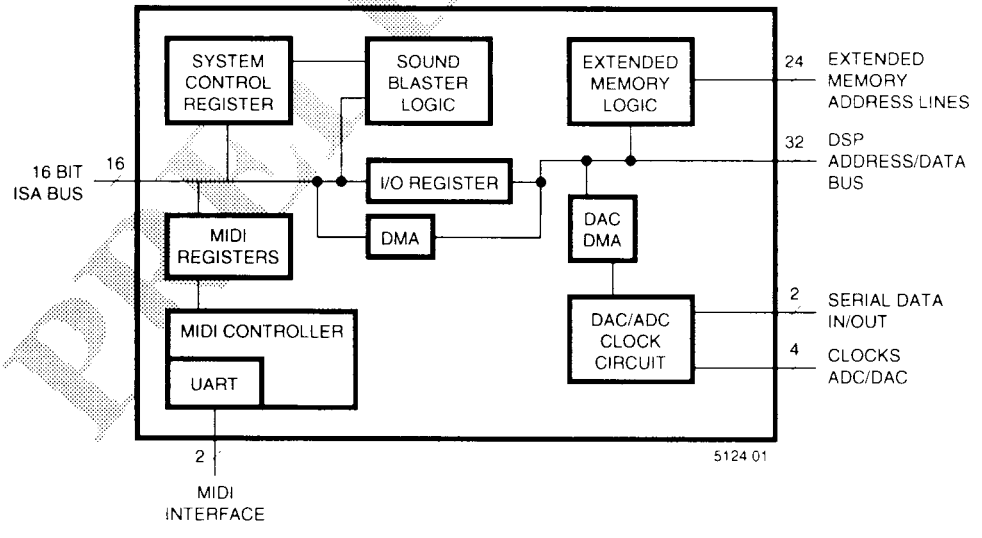
The SC18000/5 supports register level compatibility with AdLib for music generation and provide the DMA transfer logic for the 8 bit DMA transfers. This allows emulation of Sound Blaster digital audio record and playback.

The SC18005 has all the features necessary to support the Aria Synthesizer™. These include the logic for address generation of RAM or ROM of up to 16 megawords. DMA logic has been included to handle high speed 16 bit transfers. A 512 word DMA transfer space is provided in DSP memory between the audio processor (SC18025) chip and the ISA bus. In addition, another 512 word transfer area is provided for the DAC and ADC.

Both the SC18000 and the SC18005 provide the control, data, status, interface and decoding logic for the MIDI (Musical Instrument Digital Interface) port. The SC18000/5 MIDI port is similar to the industry standard Roland MPU-401 and includes smart MIDI functions such as time stamping, filtering, and intelligent merging of MIDI data.

All necessary interface logic (including serial converters) for interface to a 16 bit stereo DAC and either an 8 bit or 16 bit stereo ADC are included on chip. Recording and playback rates are selectable from 44.1 kHz, 31.5 kHz, 22.05 kHz, or 15.5 kHz. A sample rate of 11 kHz is also supported using the SC18025 audio processor chip.

BLOCK DIAGRAM



Sound Blaster and CMS are trademarks of Creative Labs Inc.
Adlib is a trademark of Adlib Inc.
MPU-401 is a trademark of Roland Corp.
Aria and Aria Synthesizer are trademarks of Sierra Semiconductor Corp.

PIN DESCRIPTIONS

All signals are CMOS compatible levels unless otherwise noted. Refer to section 3.0 for pin configuration in a 144 pin plastic quad flat pack (PQFP).

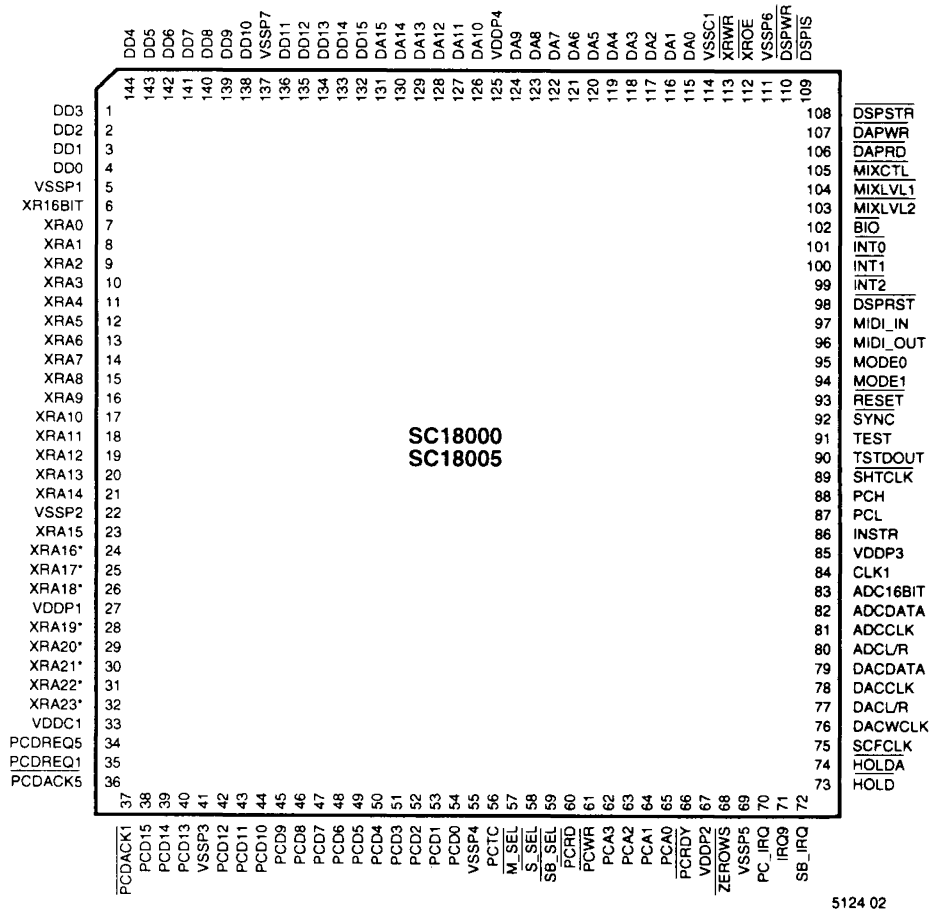
PIN NAME	PIN NUMBER		DRIVE	DESCRIPTION
	SC18000	SC18005		
ADC16BIT	83	83	input	ADC 16 bit resolution enable
ADCCLK	81	81	4mA	ADC data clock
ADCDATA	82	82	input	ADC serial data (TTL level)
ADCL/R	80	80	4mA	ADC left/right select
$\overline{BIO}$	102	102	2mA	DSP BIO signal
CLK1	84	84	input	DSP CLKOUT1 signal (10.584 MHz)
DA0–DA15	115-124, 126-131	115-124, 126-131	4mA	DSP address bus (16)
DACCLK	78	78	4mA	DAC 48x sample rate bit clock
DACDATA	79	79	4mA	DAC serial data (stereo)
DACL/R	77	77	4mA	DAC left/right clock
DACWCLK	76	76	4mA	DAC word clock
$\overline{DAPRD}$	106	106	8mA	DSP auxiliary I/O port read
$\overline{DAPWR}$	107	107	8mA	DSP auxiliary I/O port write
DD0–DD15	1-4, 132-136 138-144	1-4, 132-136 138-144	8mA	DSP data bus (16)
$\overline{DSPIS}$	109	109	2mA	DSP I/O select
$\overline{DSPRST}$	98	98	2mA	DSP reset
$\overline{DSPSTR}$	108	108		DSP Strobe
$\overline{DSPWR}$	110	110	4mA	DSP write signal
$\overline{HOLDA}$	74	74	input	DSP DMA acknowledge (grant)
$\overline{HOLD}$	73	73	2mA	DSP DMA request
$\overline{INT0}$–$\overline{INT2}$	99–101	99–101	2mA	DSP interrupts (3)
IRQ9	71	71	4mA	PC ISA MIDI interrupt
INSTR	86	86		Test Mode pin. Not connected
$\overline{M\_SEL}$	57	57	input	MIDI port select (TTL level)
MIDI_IN	97	97	input	MIDI input serial data (TTL level)
MIDI_OUT	96	96	2mA	MIDI output serial data (TTL level)
$\overline{MIXCTL}$	105	105	8mA	Analog mixer control write
$\overline{MIXLVL1}$	104	104	8mA	Analog mixer level register 1 write
$\overline{MIXLVL2}$	103	103	8mA	Analog mixer level register 2 write
MODE0–MODE1	95–94	95–94		Test Mode pin. Not connected
PC_IRQ	70	70	4mA	PC ISA ARIA interrupt
PCA0 –PCA3	62-65	62-65	input	PC ISA address bus (4) (TTL level)
PCD0– PCD15	42-54, 38-40	42-54, 38-40	4mA	PC ISA data bus (16) (TTL level)
$\overline{PCDACK1}$	37	37	input	PC ISA DMA acknowledge SB DMA 8 bit (TTL level)
$\overline{PCDACK5}$	36	36	input	PC ISA DMA acknowledge ARIA DMA 16 bit (TTL level)

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER		DRIVE	DESCRIPTION
	SC18000	SC18005		
PCDREQ1	35	35	4mA	PC ISA DMA request (8 bit DMA)
PCDREQ5	34	34	4mA	PC ISA DMA request (16 bit DMA)
$\overline{\text{PCRD}}$	60	60	input	PC ISA bus I/O read (TTL level)
$\overline{\text{PCRDY}}$	66	66	24mA	PC ISA I/O ready (wait state control) (open drain)
PCH	88	88		Test Mode pin. Not connected
PCL	87	87		Test Mode pin. Not connected
PCTC	56	56	input	PC ISA DMA terminal count (TTL level)
$\overline{\text{PCWR}}$	61	61	input	PC ISA bus I/O write (TTL level)
$\overline{\text{RESET}}$	93	93	input	Active low reset input
$\overline{\text{S\_SEL}}$	58	58	input	Sierra decoded I/O select (base address) (TTL level)
SB_IRQ	72	72	4mA	PC ISA interrupt (SoundBlaster)
$\overline{\text{SB\_SEL}}$	59	59	input	SoundBlaster emulation port select (TTL level)
$\overline{\text{SHTCLK}}$	89	89		Test Mode pin. Not connected
SCFCLK	75	75	2mA	Switched capacitor filter clock
$\overline{\text{SYNC}}$	92	92		Test Mode pin. Not connected
TEST	91	91		Test Mode pin. Not connected
TSTDOUT	90	90		Test Mode pin. Not connected
VDDP1–VDDP4, VDDC1	27, 67, 85, 125, 33	27, 67, 85 125, 33	input	+5 volts VCC (5)
VSSP1–VSSP7, VSSC1	5, 22, 41, 55, 69, 111 137, 114	5, 22, 41, 55, 69, 111 137, 114	input	Digital core and pad ring ground (8)
XR16BIT	6	6	input	Extended memory 16 bit width enable (TTL level)
XRA0–XRA23	7-21, 23	7-21, 23-26 28-32	2mA	ROM/RAM extended memory address outputs (24) ** note: the SC18000 has only XRA0 to XRA15 outputs
$\overline{\text{XROE}}$	112	112	8mA	Extended ROM/RAM buffer output enable (RD or WR)
$\overline{\text{XRWR}}$	113	113	8mA	Extended memory RAM write
$\overline{\text{ZEROWS}}$	68	68	24mA	PC ISA zero wait state enable (open drain)

CONNECTION DIAGRAM

The SC18000 and SC18005 are each available in a 144 pin quad flat package. The SC18005 is a superset of the SC18000 with the capability to address 16 Mwords (rather than 64 kwords) of extended ROM/RAM space (pins marked * are not connected on the SC18000).



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*THESE PINS UNCONNECTED ON SC18000

REGISTER ADDRESSING

There are a number of internal registers in the SC1800X for system control, MIDI interface, Sound Blaster emulation, and DSP registers.

ISA system registers

There are four write only and three read only 16 bit system registers accessible to the ISA bus in the SC1800X chip.

OFFSET FROM BASE	READ	WRITE
0	(from) DSP data port	(to) DSP data port
2	system status	system control
4	N/A	DMA/DA transfer base address
6	DA transfer data port	DA transfer data port

The DSP data port consists of two 16 bit registers, one for data transfer in each direction from ISA bus to/from the DSP. After reset, the DMA/DA transfer base address defaults to $7C00, and the control port to $0040. The system control port bits are as follows:

CONTROL PORT BIT	FUNCTION
0	Enable interrupt of ISA after DSP data port read (PC_IRQ)
1	Enable interrupt of ISA after DSP data port write (PC_IRQ)
2	Enable interrupt of DSP after ISA data port read (INT2B)
3	Enable interrupt of DSP after ISA data port write (INT2B)
4	Enable interrupt of ISA after ISA DMA terminal count signal (PC_IRQ)
5,6	Select sample rate: 00=44.1, 01=22.05, 10=31.5, 11=15.75kHz
7	Aria (1)/Sound Blaster (0) mode select
8	Hold DSP in reset state
9	DMA transfer direction: 1=DSP to ISA, 0=ISA to DSP
10	Initiate DMA transfer (ISA to/from DSP)
11-15	Reserved: these bits must be set to 0

The system status port is an echo of the control port with the following exceptions:

STATUS PORT BIT	FUNCTION
10	(1) Indicates DMA transfer in progress
15	(1) Data port busy: indicates DSP has not read from data port

DMA (Direct Memory Access) and DA (Direct Access) transfers are set up to start at an address in DSP memory determined by the 16 bit transfer base address register. The lower 9 bits of this location are a counter which automatically increments after each transfer. 'Direct access' refers to the technique of reading or writing a single location of DSP memory at a time using ISA bus I/O accesses of the DA transfer port register, which acts like a single word 'window' into DSP memory. DA uses the transfer base address register and counter in the same way DMA does.

MIDI registers

The address base of the MIDI port is set by external decoding logic, and is usually set to 330 hex. These registers are 8 bits wide except for the status port which has only bits 6 and 7 defined. Bit 7 (when LOW) indicates data is available in the MIDI IN register (and generates IRQ9), and bit 6 (when LOW) indicates that the MIDI OUT register is empty and ready for transmitting data .

OFFSET FROM BASE	READ	WRITE
0	MIDI in data	MIDI out data
1	MIDI status	MIDI command

These registers are also accessible by the COP880 microcontroller in its data memory area, as well as the registers for communicating with the DSP. See section 5.8 for addressing information.

Sound Blaster registers

The Sound Blaster registers support emulated FM synthesis and 8 bit PCM output or input. The C/MS chips, Sound Blaster MIDI, data compression/decompression, and game port are not emulated. These registers are 8 bits wide, and their base address is set by external decoding logic on any 16 byte boundary in ISA I/O space. Default base address should be 220 hex, but note that the synthesis registers are normally also accessible at 388/389 hex. Note that these registers are only valid when the ISA system control register bit 7 is '0' (mode select - see 4.1). The 'Digital Sound Processor' status registers have only bit 7 defined.

OFFSET FROM BASE (HEX)	READ	WRITE
6	NA	system reset
8	Synthesis status	Synthesis register address
9	NA	Synthesis data
A	'DSP' data	NA
C	'DSP' write buf status	'DSP' data
E	'DSP' data avail status	NA

DSP registers

There are several registers internal to the SC1800X chip accessible to the DSP in its I/O space. These are all 16 bits wide, except that the extended ROM and RAM data spaces may be 8 or 16 bits wide. The ROM and RAM referred to in this table are the EXTENDED ROM and EXTENDED RAM (limited to 64k on the SC18000). The address space from 0 to 7 is reserved for internal registers, and the remaining space from 8 to F is used for external mixer and auxiliary circuitry (such as telephone line interface) control. $\overline{\text{MIXLVL1}}$, $\overline{\text{MIXLVL2}}$, $\overline{\text{MIXCTL}}$, $\overline{\text{DAPRD}}$ (DSP auxiliary port read), and $\overline{\text{DAPWR}}$ are active low outputs for this external analog logic.

OFFSET FROM BASE (HEX)	READ	WRITE
0	(from) ISA data port	(to) ISA data port
1	DSP status register	DSP control register
2	N/A	DAC and ADC DMA base address
3	(from) SB data port (lower 8 bits only)	(to) SB data port (lower 8 bits only)
4	N/A	ROM page and mask size select
5	ROM/RAM data	RAM TABLE data
6	Test register	N/A
7	MIDI interconnect	MIDI interconnect (8 bit registers in low byte)
8,9	N/A	$\overline{\text{MIXLVL1}}$
A,B	N/A	$\overline{\text{MIXLVL2}}$
C,D	N/A	$\overline{\text{MIXCTL}}$
E,F	$\overline{\text{DAPRD}}$	$\overline{\text{DAPWR}}$

The DAC/ADC base address defaults to $7E00 after reset.
The DSP control and status registers are 10 bit ports with bit positions configured as follows:

BIT	STATUS (READ)	CONTROL (WRITE)
0	SB Interrupt State	Generate SB interrupt (pulsed)
1	DMA incomplete (1)	Initiate DMA block transfer
2	DMA direction	DMA direction (0) PC to DSP, (1) DSP to PC
3	SB Data Port Busy	N/A
4	SB DMA burst incomplete	Initiate SB DMA burst transfer
5	ADC disabled	ADC disable (1)
6	SB DMA Terminal count interrupt enable	SB DMA terminal count interrupt enable
7	System reset state	system reset (pulsed)
8	(1) Aria (0) SB emu. status	N/A
9	SB 'DSP' Write Buffer Busy Flag	N/A

The system reset control bit resets bits 0-7 of the ISA bus control port and resets the ISA bus DMA/DA base address counter to its default of $7C00. DMA transfers can be triggered by either the ISA bus or the DSP from the initiate DMA transfer bit. SB DMA transfers occur in bursts of 16, with each burst being triggered with bit 4. When in SB mode (see the PC control register bit 7) the DMA direction is controlled by the DSP control register bit 2, and in Aria mode the DMA direction is controlled by the ISA bus control register.

Extended Memory Addressing

The extended address generation logic (64KW on SC18000, 16MW on SC18005) is designed for easy wave table lookups by the DSP. This logic not only provides extended address outputs, but also includes masking circuitry to limit DSP accesses to a specific table size. The page and mask size select registers are programmed as follows:

REGISTER BITS	FUNCTION
0-2	Mask size select: (bits 2-1-0)
3-7	ROM/RAM address bits XRA16 to XRA20
8-10	Table base offset bits XRA8 to XRA10 (if masked, these bits provide address outputs XRA21 to XRA23)
11-15	Table base offset bits XRA11 to XRA15 (if masked, these bits are don't care, and should be set to zero)

Mask size selections: (bits 2,1,0): Bits valid for base address (bits 15 to 8):

Selection	Table Size	2, 1, 0	15	14	13	12	11	10	9	8
0	256 word	000	x	x	x	x	x	x	x	x
1	512 word	001	x	x	x	x	x	x	x	*
2	1k	010	x	x	x	x	x	x	*	*
3	2k	011	x	x	x	x	x	*	*	*
4	4k	100	x	x	x	x	–	*	*	*
5	8k	101	x	x	x	–	–	*	*	*
6	16k	110	x	x	–	–	–	*	*	*
7	64k	111	–	–	–	–	–	*	*	*

x valid table base address bit
* extended address output A23–A21
– don't care (should be set to zero)
Note that there is no 32k word table size selection.

The extended ROM/ RAM address bits XRA21, XRA22, and XRA23 are generated by making use of bits 8,9 and 10 only when they are masked out (i.e. unused) by the settings of bits 0,1 and 2. This limits the minimum table size in the upper segments of extended memory as follows:

ADDRESS RANGE	XRA23	XRA22	XRA21	TABLE SIZE SELECTABLE
0 to 2M	0	0	0	256 to 64k
2M to 4M	0	0	D8	512 to 64k
4M to 8M	0	D9	D8	1k to 64k
8M to 16M	D10	D9	D8	2k to 64k

The procedure for using this circuitry is a three step process. First, the base address and table size settings are stored in the base/mask register using an OUT instruction (to port #4) from the DSP. Second the lookup table base address must be calculated and stored in a predefined area of external memory ($6080 to $60BF). The extended address logic reads the address from the data bus while the write is being performed, and performs the selected masking function. The DSP must then wait for the ROM to access - 50ns plus ROM maximum access time - total 250ns. This will require waiting a minimum of two instruction cycles (since a one cycle delay is already between the store and the IN), however useful processing may be done during this interval. Third, the extended memory at the selected address may then be read using an IN from the data port (#5) or written to (if it is RAM) by using an OUT to the data port. The data throughput may be increased by looking up several samples at a time from the same table - then the first step (OUT to base/mask register) is only done once at the beginning of the procedure.

INTERNAL LOGIC SPECIFICATION

This section describes in detail the internal logic and timing requirements of all sections of the SC1800X. All timing specifications apply over the full range of operating conditions.

OPERATING CONDITIONS	MIN	MAX	UNITS
Supply voltage $V_{DD} - V_{SS}$	4.75	5.25	V
Voltage on any pin	-0.5	V_{DD}	V
Operating temperature range	0	+70	degrees C
TTL input logic low	-0.5	0.8	V
TTL input logic high	2.0	V_{DD}	V
CMOS input logic low	-0.5	$0.3*V_{DD}$	V
CMOS input logic high	$0.7*V_{DD}$	V_{DD}	V
output logic low	0	0.4	V at max. load
output logic high	2.4	V_{DD}	V at max. load
Capacitive loading: (maximum to meet specifications)	ISA bus outputs	100	pF
	other bus outputs	50	pF
	standard outputs	15	pF

ISA BUS PORT DECODING

This logic decodes the ISA bus I/O port locations for the SC1800X internal registers. Separate blocks of decoding are provided for the 16 bit Sierra, the 8 bit MIDI, and the 8 bit Sound Blaster ports. An external PAL or other logic is required to decode the base address of each of these blocks, allowing flexibility in placing these blocks of registers. Only the lower ten address lines need to be decoded for the port addresses on the ISA bus. The PAL must decode the bus address and qualify it with bus signal AEN low and provide the 16BITIO signal to the ISA bus for the Sierra ports and the Sound Blaster ports (internally treated as 16 bit ports.) The SC1800X internally qualifies I/O port reads and writes using the $\overline{PCRD}$ and $\overline{PCWR}$ signals. The SC1800X internal logic provides internal register select lines, and the ISA bus $\overline{ZEROWS}$ and PCIORDY outputs.

Recommended external PAL address decoding:

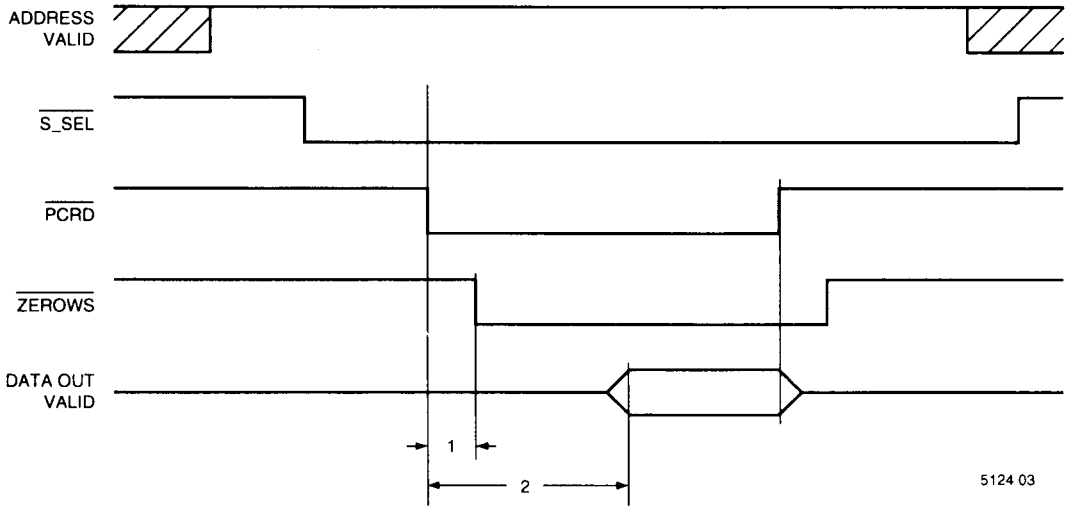
OUTPUTS:	INPUTS:		
Pin active (L)	AEN	A10 - A4	A3
$\overline{S\_SEL}$	L	$29	X
$\overline{M\_SEL}$	L	$33	0
$\overline{SB\_SEL}$	L	$22	X
$\overline{SB\_SEL}$	L	$38	1
16BITIO	L	$29	X
16BITIO	L	$22	X
16BITIO	L	$38	1

NOTE 1: The PAL should be 25ns or faster.

NOTE 2: The indicated port decode locations are for default bases. Adding different (selectable) base addresses will alter the decode spaces.

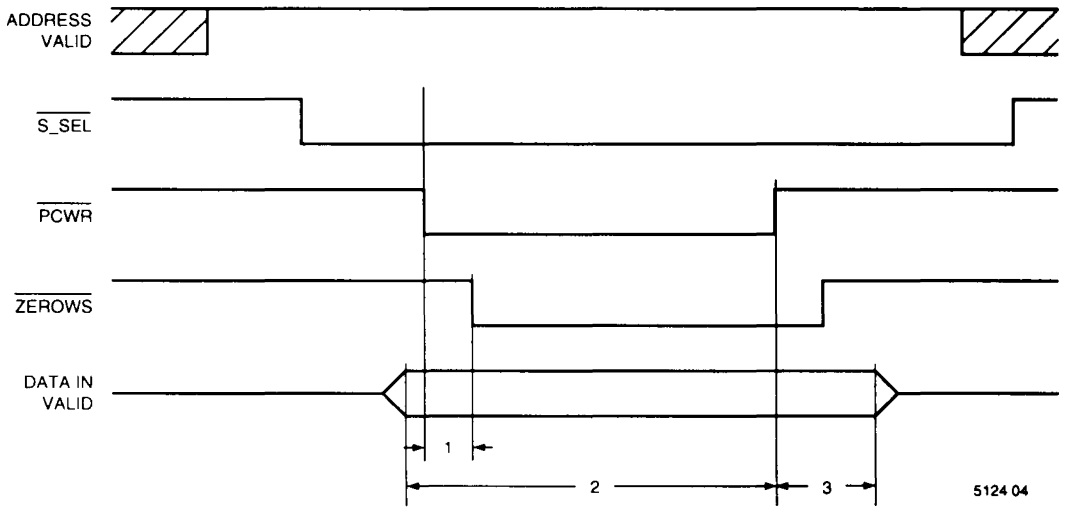
The SC18000 provides the $\overline{ZEROWS}$ output to the ISA bus, which allows zero wait state access to all ports (except during Direct Access and DMA transfers).

Timing for ISA bus access to the SC1800X internal registers:



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{ZL}	$\overline{ZEROWS}$ active from $\overline{IORD}$ or $\overline{IOWR}$			25	ns
2	t_{DV}	Internal data available from $\overline{IORD}$			50	ns

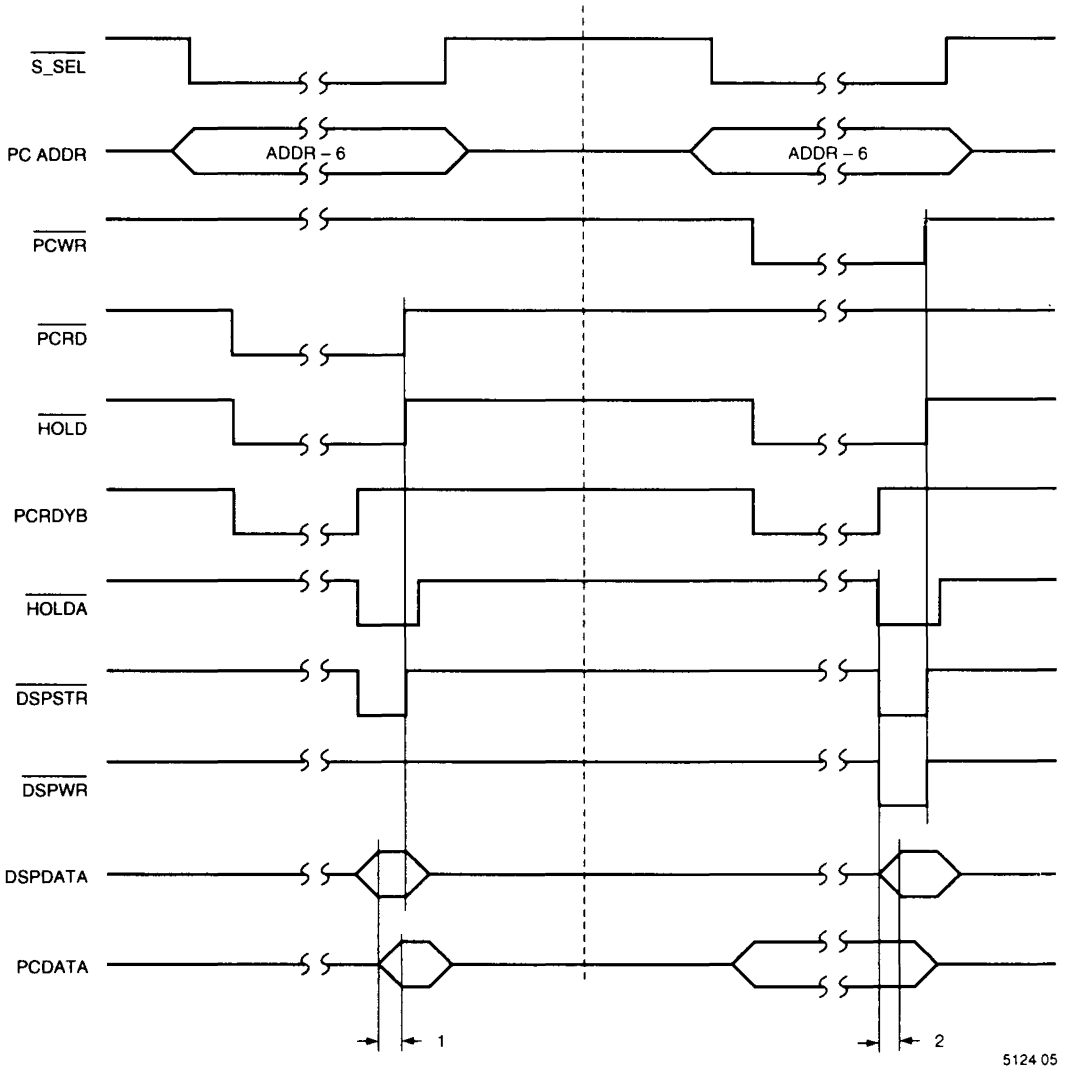
Figure 2. ISA Bus Read



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{ZL}	ZEROWS active from IORD or IOWR			25	ns
2	t_{DV}	Data valid from IOWR	106			ns
3	t_{DI}	Data hold from IOWR	35			ns

Figure 3. ISA Bus Write

Timing for Direct Access to DSP memory is slightly different than ISA bus access to the SC1800X internal registers. The PCRDY signal is used to insert wait states on the ISA bus until the DSP hold acknowledge (HOLDA) goes active. Note that the breaks in the following diagrams reflect the unknown delay between a hold request (HOLD) and a hold acknowledge (HOLDA) from the DSP.



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{PDA}	ISA bus data valid from DSP data valid			50	ns
2	t_{DDA}	DSP data valid from $\overline{DSPSTR}$ valid			10	ns

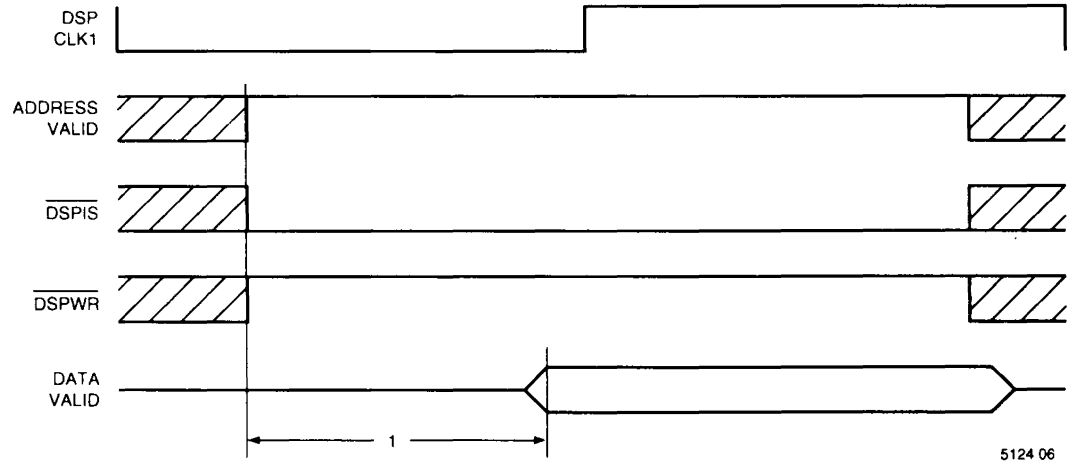
Figure 4.

DSP PORT DECODING

The DSP I/O port decoding logic provides register select lines for both on chip and off chip registers.

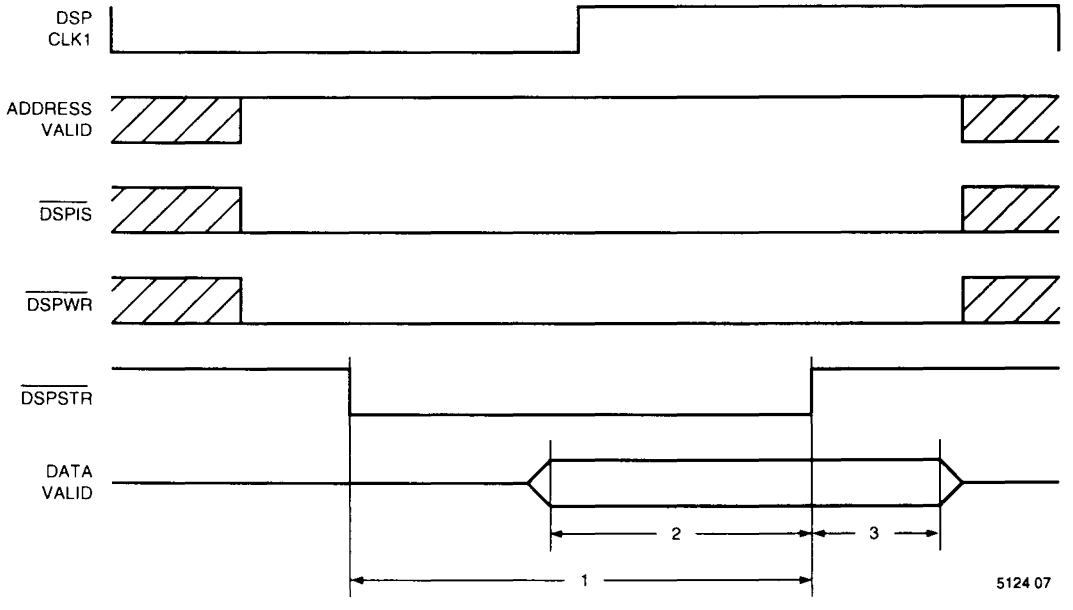
Zero wait state timing for all DSP accesses is provided.

DSP access to SC1800X internal registers is as follows:



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DV}	Data valid from $\overline{DSPIS}$			31	ns

Figure 5. DSP Read



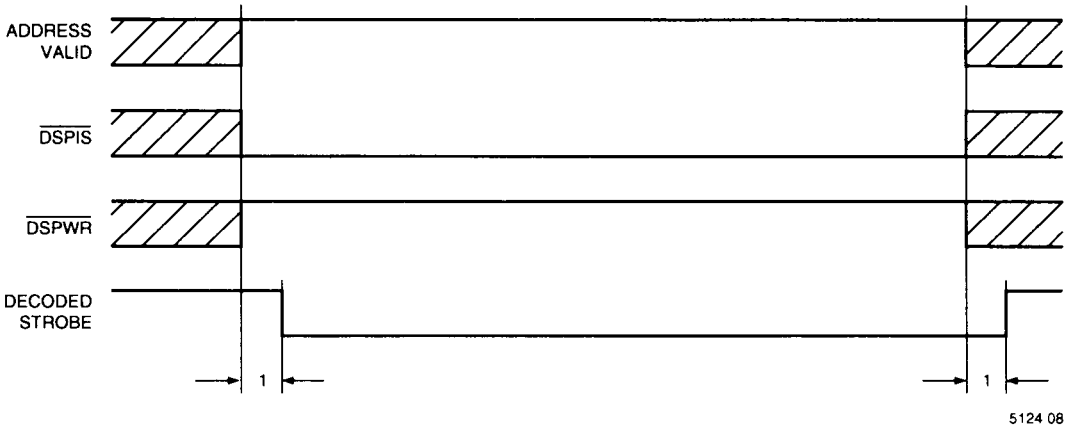
NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{STR}	$\overline{DSPSTR}$ pulse width	42			ns
2	t_{DV}	Data valid from $\overline{DSPSTR}$ high	27			ns
3	t_{DI}	Data hold from $\overline{DSPSTR}$ high	14			ns

Figure 6. DSP Write

The SC1800X also decodes strobes for the following external port accesses:

EXTERNAL SELECT OUTPUT ACTIVE:	INPUTS: $\overline{DSPWR}$	$\overline{DSPIS}$	$\overline{DSPSTR}$	DSP ADDRESS A3	A2	A1	A0	DIAGRAM
$\overline{MIXLVL1}$	L	L	L	1	0	0	x	P2
$\overline{MIXLVL2}$	L	L	L	1	0	1	x	P2
$\overline{MIXCTL}$	L	L	L	1	1	0	x	P2
$\overline{DAPWR}$	L	L	L	1	1	1	x	P2
$\overline{DAPRD}$	H	L	X	1	1	1	x	P1
$\overline{XRWR}$	L	L	L	0	1	0	1	P3
$\overline{XROE}$	X	L	X	0	1	0	1	P3

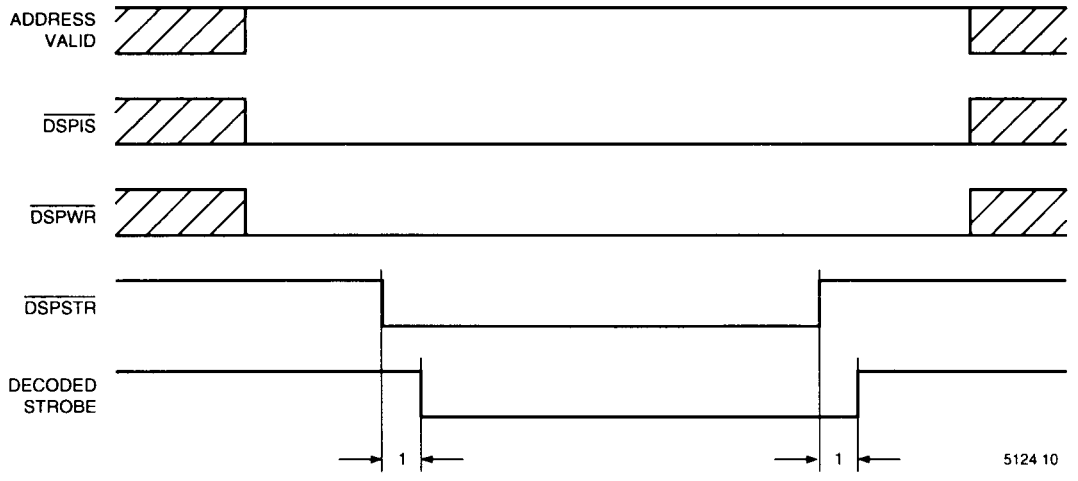
The timing on decoded external port reads is as follows: P1



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DS}	Strobe delay from $\overline{DSPIS}$ edge			14	ns

Figure 7.

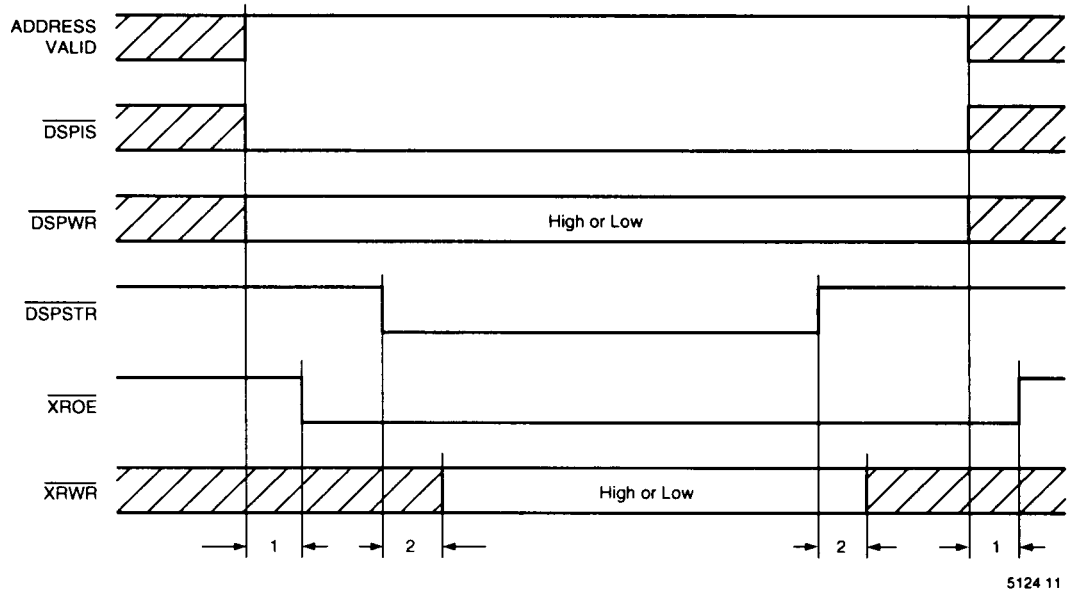
The timing on decoded external port writes is as follows: P2



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DS}	Strobe delay from $\overline{DSPSTR}$ edge			12	ns

Figure 8.

The timing on the External ROM decoded strobes ($\overline{XROE}$ and $\overline{XRWR}$) is as follows: P3



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{OE}	$\overline{XROE}$ delay from $\overline{DSPIS}$ edge			14	ns
2	t_{WR}	$\overline{XRWR}$ delay from $\overline{DSPSTR}$ edge			12	ns

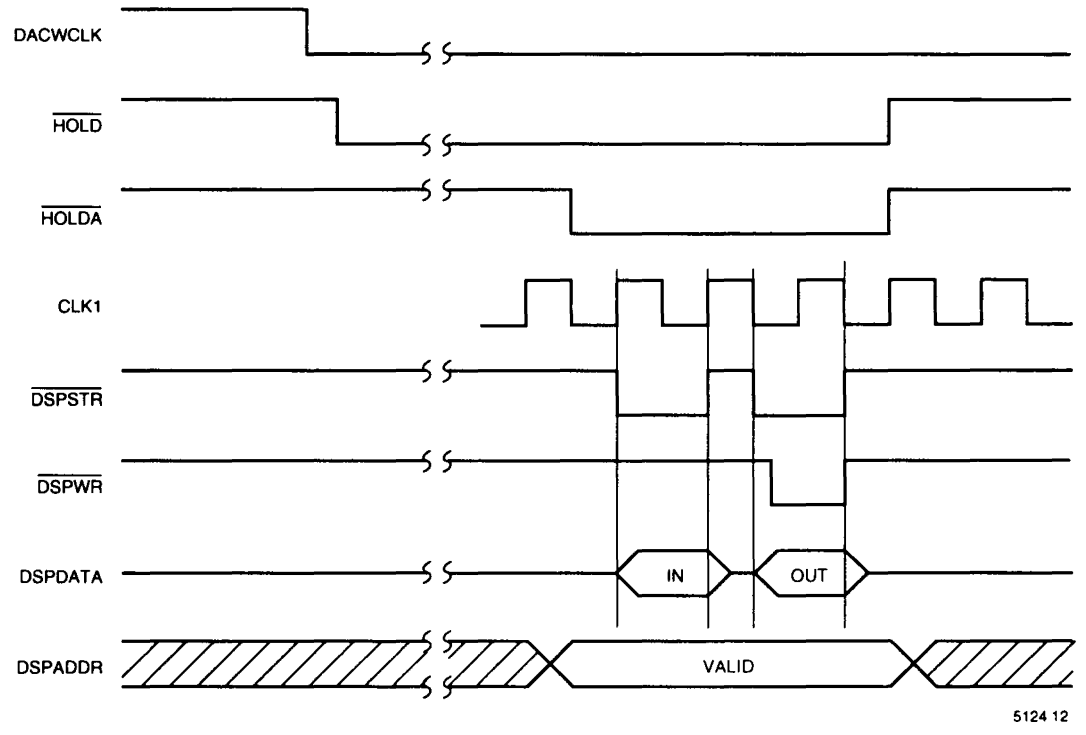
Figure 9.

DMA CONTROLLER

The SC1800X DMA controller interfaces the DSP bus to three sources/destinations of data—the ISA bus, the DAC, and the ADC. Each system may be transferring data simultaneously, so the controller arbitrates the DMA requests by delaying processing of DMA requests until the controller is free. The DMA controller also generates appropriate DSP bus addresses, ISA DMA requests, DSP bus requests, and DSP bus control strobes required for the transfer before returning the system to normal operation. The ISA bus DMA transfers may be either 16 bit (Aria mode) or 8 bit (Sound Blaster mode) depending upon the setting of bit 7 in the control register.

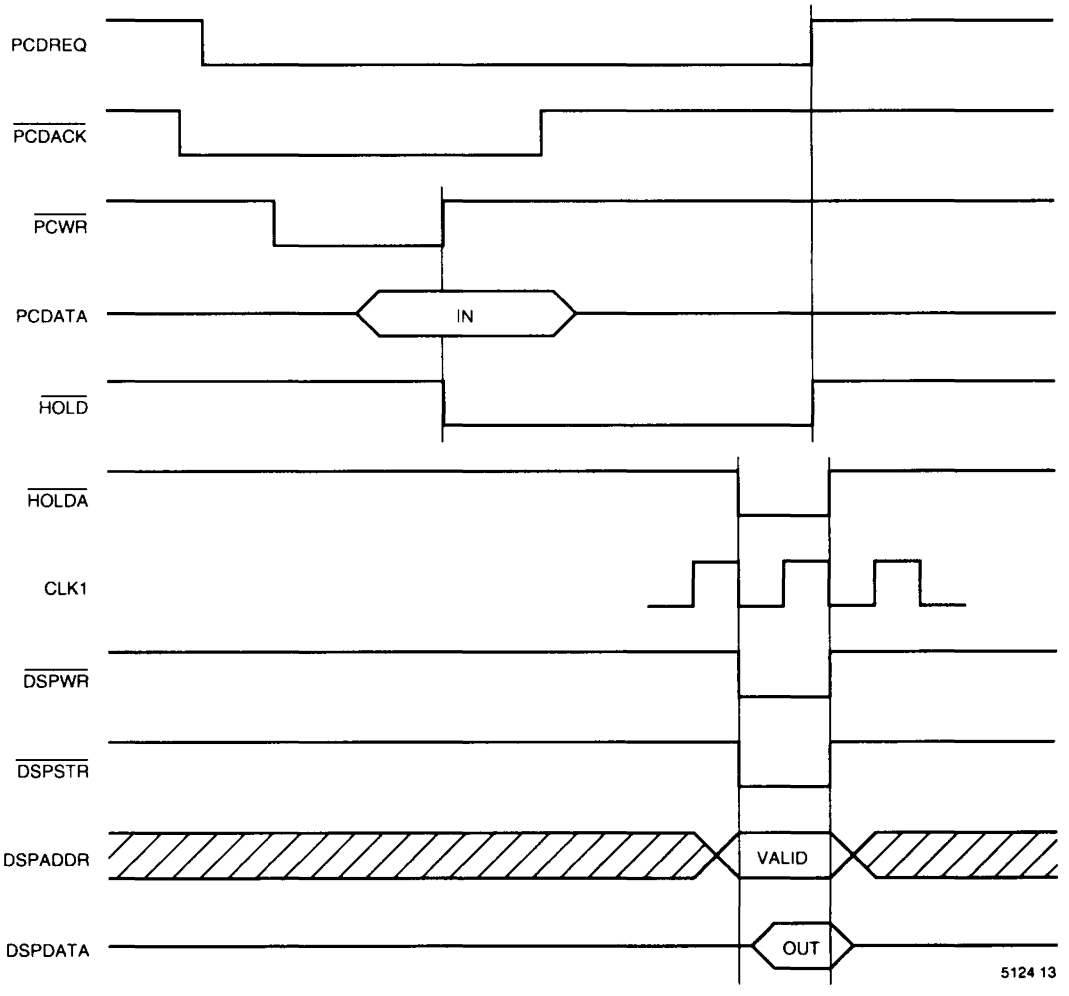
After $\overline{RESET}$ is released, the DAC/ADC transfer is enabled and will begin occurring (starting from DSP memory address $7E00). Thereafter transfers occur each half sample period, alternating left samples from even memory locations and right samples from odd memory locations. The DAC/ADC transfers occur irrespective of the DSP state, and will still occur even when the DSP is in reset (bit 8 of control register). The DAC and ADC transfers are tied together to the overall system sample rate and transfer to and from the same area of memory, allowing one address counter and associated control logic to be used for both. The DMA controller first does a transfer from DSP memory to the DAC, emptying the DSP memory cell. Then, if the ADC is enabled via bit 5 of the DSP control register, the DMA controller transfers one word of data from the ADC into the same DSP memory cell just emptied . When the ADC is in 8 bit mode its data is stored in the most significant byte of DSP memory, with the lower byte zeroed. Thus the same area of DSP memory is used as both the input and output FIFO of the system. Finally, the DSP is interrupted at the mid-point and the end-point of the DAC/ADC transfer FIFO (base+256 words and base+512 words respectively) to allow the DSP to process the ADC samples received and to fill the memory with the next block of DAC samples.

DAC/ADC DMA TRANSFERS:



ISA DMA block transfers are initiated at the request of the host computer, which involves several steps. First the host sets up its own DMA controller (transfer addresses, length count, control bits), then sets the SC1800X control register bits 4 and 9 (terminal count interrupt and transfer direction) as well as the SC1800X transfer base address register. Finally, bit 10 of the SC1800X control register is set high to initiate the DMA transfer (Aria mode only). This bit should only be written high once to initiate each DMA block transfer. Thereafter only zeros should be written to this bit. When the block transfer is complete, bit 10 of the status register will go low, and the host will be interrupted if bit 4 of the control register was set.

ISA BUS DMA TRANSFERS



DMA transfers in Sound Blaster mode are slightly different in that they are 8 bit and do not require the use of the SC18000X control register DMA bits, as the DSP automatically controls the ISA terminal count interrupt, the transfer direction, and DMA initiating via the DSP control register. SB DMA is also done in bursts of 16 transfers, with each transfer being initiated from the DSP control register and the DSP being interrupted at the end of each burst.

DMA ADDRESS GENERATOR

This logic consists of two sections, one for ISA bus DMA and DA transfers, and one for DAC and ADC transfers. Each section contains a loadable 9 bit counter at the least significant bit positions, and a 7 bit latch in the upper bit positions, with the ISA transfer register loadable from the ISA bus while the DAC/ADC transfer register is loadable from the DSP bus. These counters allow 512 word transfer areas to be set up on any 512 word boundary in memory. After application of the external reset ($\overline{\text{RESET}}$) signal, the ISA DMA register/counter is set to $7C00, and the DAC/ADC DMA register/counter is set to $7E00. The ISA DMA register is also resettable to $7C00 by generating a system reset via bit 7 of the DSP control register. The counters advance automatically after each ISA word transfer and after each DAC/ADC combined word transfer and loop automatically from 1FF to 000. A DSP interrupt INT0 is automatically generated at the 256 and 512 word boundaries of the DAC/ADC counter.

DAC AND ADC TIMING

The DAC, switched capacitor filter, and ADC clocks are derived from the single clock input CLK1 at 10.584MHz. Four (stereo) system sample rates are selectable: 44.1kHz, 31.5kHz, 22.05kHz, and 15.75kHz.

The DAC clock signals consist of a bit clock (48X the sample rate) , a word clock (2X the sample rate), and a left/right clock (1X the sample rate.) Samples are organized in memory with left samples at even addresses, and right samples at odd addresses. The ADC operates at the same clock frequency and sample rate as the DAC, but its bit clock is gated in bursts of 8 or 16 cycles depending on sample size selected by the ADC16BIT input. A switched capacitor filter clock output which tracks the DAC/ADC sample rate is provided at 1/3 of the bit clock rate (50% duty cycle).

Clock outputs with CLK1 = 10.584MHz

OUTPUT	FREQUENCY (KHz)				
	FS = 44.1	31.50	22.05	15.75	
DACCLK	2116.8	1512.0	1058.4	756.0	50% duty cycle
DACWCLK	88.2	63.0	44.1	31.5	33% duty cycle
DACL/R	44.1	31 .5	22.05	15.75	50% duty cycle
ADCCLK	2116.8	1512.0	1058.4	756.0	gated - 8 or 16 clocks
ADCL/R	44.1	31.5	22.05	15.75	50% duty cycle
SCFCLK	705.6	504	352.8	252	50% duty cycle
50x filter Fc	14.11	10.08	7.056	5.04	cutoff frequency

Timing specifications:

Clock skew, DACCLK to DACWCLK or DACL/R	25ns max
Clock skew, DACCLK to ADCCLK or ADCL/R	25ns max

DAC and ADC data is valid on the rising edge of the bit clock (DACCLK, ADCCLK), and changes on the falling edge. DACWCLK indicates completion of a left or a right word transfer cycle on its falling edge, and DACL/R (also ADCL/R) are high for left channel, low for right channel data. The burst of ADCCLK cycles occurs 4 bit clock cycles after each ADCL/R transition (high or low). A stereo transfer is complete in 48 DAC bit clock cycles, and the next transfer begins immediately.

The following diagram shows all external clock signals over a single sample period. ADC clock and data signals are shown for both 8 and 16 bit modes of operation. ADC data "don't care" times are shown shaded.

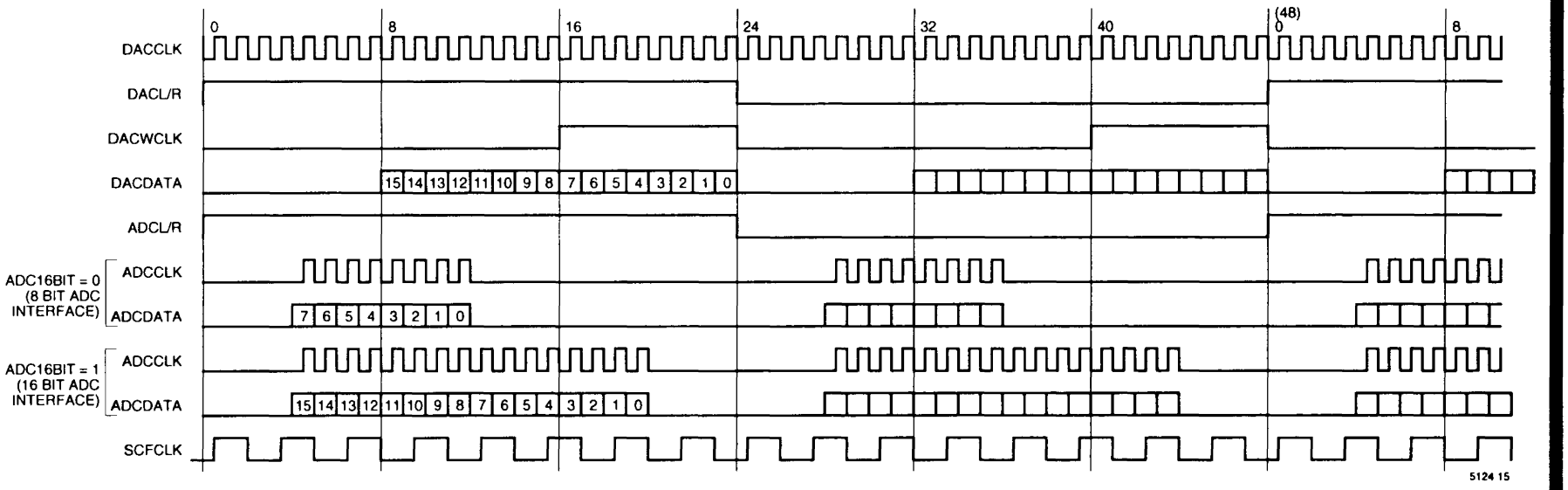


Figure 10. DAC and ADC Timing Signal

SYSTEM CONTROL

This circuit handles interrupt generation, mode select bits, and DMA control bits. This register defaults to $0040 on reset, enabling Sound Blaster emulation as the default setting. The bit settings may be changed by an ISA bus I/O port write cycle to the control register address. See ISA system register section for a description of the control bits in this register. Bits 7–0 of this register a re also reset to their defaults from the DSP control port (bit 7).

SOUND BLASTER INTERFACE

This logic provides an emulation mode for Sound Blaster synthesis, 8 bit DAC, and ADC interface. The CMS™ chip, Sound Blaster MIDI port, composite speech mode, and Sound Blaster compression formats are not supported. This is the default mode on power-up . When in emulation mode, the Sierra ISA bus DMA and data registers should not be used. The Sierra control register can still be accessed, but in order for the Sound Blaster emulation to work properly the control bits should not be changed from their default settings.

The SC1800X treats the Sound Blaster registers as 16 bit ports, even though the true Sound Blaster is an 8 bit card. During reads of all (valid) ISA ports the upper byte is returned as undefined. During DSP reads of the Data/Command Buffer data the upper byte is also undefined, but the DSP reads the two Synthesis registers as one 16 bit value as described in a following paragraph. The following Sound Blaster registers are emulated:

	READ:	WRITE:
Base + 6		Sound Blaster Reset
Base + 8	Synthesis Status	Synthesis Register Select
Base + 9		Synthesis Data
Base + A	Read Data (from DSP)	
Base + C	Write Buffer Status (bit7)	Data/Command Buffer
Base + E	Data Available Status (bit7)	

Writing a one to the Sound Blaster reset port initiates a Sound Blaster reset sequence. Any other value brings the DSP out of RESET and is also echoed back (inverted) at the Read Data port (Base + A).

The Synthesis registers are actually Adlib compatible registers, also accessible from hex 388 and 389 on the ISA bus. Since the Sound Blaster emulation treats all registers as 16 bits wide, the ISA bus automatically re-routes 8 bit ISA writes to the Synthesis Data register (base + 9) to the upper 8 bits of the ISA bus. When in Sound Blaster mode, the SC1800X therefore captures writes to the Synthesis Register Select port in the lower 8 bits of DSP port 0 and writes to the Synthesis Data port in the upper 8 bits of DSP port 0; supplying the two together to the DSP when it reads the DSP I/O port 0 (in Sound Blaster mode.) The DSP is also interrupted on interrupt 2 whenever the Synthesis Data port is written to. The lower 8 bits from DSP writes to I/O port 0 are also captured by the SC1800X (when in Sound Blaster mode) and are supplied to the ISA bus when the Synthesis Status port is read (Base + 8).

The Read Data register is an 8 bit register that is written to by the DSP at I/O port 3 (lower byte) and is read by the ISA bus from Base + A. DSP writes to I/O port 3 also set the Data Available Status bit (bit 7 of the port Base + E) which is then cleared by ISA reads of port Base + A.

The Data/Command Buffer is an 8 bit register written to from the ISA bus and read by the DSP from I/O port 3 (lower byte). Writes from the ISA bus to port Base + C also set bit 7 of the Write Buffer Status register as well as generate a DSP interrupt 2. DSP reads of I/O port 3 clear bit 7 of the Write Buffer Status register.

MIDI INTERFACE

An internal COP880 microcontroller provides a MPU-401 compatible MIDI interface. A subset of the MPU-401 commands is implemented, and the bus registers are identical to the MPU-401.

The COP880 has 192 bytes of RAM and 2k bytes of ROM, and is clocked from CLK1 at 10.584 MHz giving an instruction cycle time of 0.945 µs. Added to this core are registers for communications with the ISA bus, and a UART for the serial MIDI interface. The MIDI specification requires a baud rate of 31.25 kbps (±1%) with one start, 8 data, one stop bit, and no parity. The UART requires a 16x clock source—500 kHz ±5 kHz to be within this specification. CLK1 is divided by 21 to produce 504 kHz (31.5 kbps) for the UART.

The ISA bus address base of the MIDI port is set by external decoding logic, and is usually set to 330 hex. These registers are 8 bits wide except for the status port which has only bits 6 and 7 defined. Bit 7 (when LOW) indicates data is available in the MIDI IN register (and generates IRQ9), and bit 6 (when LOW) indicates that the MIDI OUT register is empty and ready for transmitting data.

Offset from base	READ	WRITE
0	MIDI in data	MIDI out data
1	MIDI status	MIDI command

Status register bits:

BIT #	Description	ISA BUS INTERRUPT	
0-5	not used		
6	DRRB	none	This bit is set high by an ISA bus write to the MIDI out data or command port (offset 0 or 1), and reset low by a microcontroller read of these ports.
7	DSRB	IRQ9	This bit is reset low by a microcontroller write to the data port, and set high by an ISA bus read of the MIDI in data port at offset 0. The interrupt is positive edge triggered (on the microcontroller write to this port).

MIDI COMMAND SUPPORT

This list describes commands supported by the MIDI microcontroller firmware. This revision is intended to be used in UART, DATA IN STOP, or RECORD modes only. Exact MPU 401 emulation is implemented ONLY in UART mode. Major differences between this firmware and the MPU401 are:

- THRU data is not supported.
- Channel reference tables are not used.
- There are no selectable filters on MIDI input data, all commands except F8, FE, and FF are passed from MIDI input to host.
- Play tracks are not supported, all output data is sent using 'Want To Send Data/System' commands, with track information ignored. (No separate running status is kept for each channel)
- Metronome is not supported.
- No MIDI real time messages are sent to the MIDI OUT port unless transmitted by the Want To Send System command. (F8, FA, FB, FC)
- Conductor mode is not supported.

The following commands are supported:

Note that the software sending any of these commands must always receive the ACK byte ($FE) sent in response. The only time the board does not send an ACK in response to a command is a RESET ($FF) sent while the board is in UART mode.

COMMAND (HEXADECIMAL)	DESCRIPTION
11	STOP RECORD - stops time stamped recording which was started with command 22. The MIDI message for stop (FC) is not sent by this command.
22	START RECORD - starts time stamped recording. All commands received from the MIDI interface are filtered (certain messages are not passed to the host) and preceded with a timing byte. The value of the timing byte is the difference in time from the last message received, in units determined by TEMPO and TIMEBASE settings. A timing byte of F8 is sent if the record counter overflows, this value should be interpreted as 240 decimal. The timing byte precedes running status bytes as well. Note that the MIDI message for start (FA) is not sent by this command.
34	With timing byte in data in stop mode - sends a zero timing byte ahead of data when in data in stop mode.
3F	Sets interface into UART mode. In this mode, MIDI data is passed unaltered in both directions from the interface. All commands except RESET are ignored.
8A	Data in stop OFF.
8B	Data in stop ON - allows reception of data from MIDI without time stamp bytes. If command 34 is used, a dummy zero timing byte is sent. Data received in this mode is filtered as if in record mode.
AB	Read and clear record counter. The return value is added to the input data stream immediately after the ACK (FE); this applies to any other command that returns data in response.
AC	Read software version (returns $15 to emulate MPU 401).
AD	Read software revision (returns $01).
AF	Read TEMPO setting.
BA	Clear record counter.
C2 - C8	Set TIMEBASE in 'ticks per beat': Command: C2 C3 C4 C5 C6 C7 C8 Timebase 48 72 96 120 144 168 192 Max Tempo 240 240 240 240 208 179 179 Min Tempo 32 16 16 8 8 8 8
D0	Want To Send Data (WSD)
DF	Want To Send System message - these two commands allow any data following on the MIDI data port to be transmitted to MIDI out until any other command from the host is received. No time stamp byte is required or needed, data is sent immediately as it is received from the host.
E0	Set TEMPO in beats per minute (8 to 240).
FF	RESET interface - all parameters are set to power on defaults.

EXTENDED ROM/RAM ADDRESS GENERATION

The extended address generation logic (64k on SC18000, 16M on SC18005) is designed for easy wave table lookups by the DSP. This logic provides extended address outputs, and includes masking circuitry to limit DSP accesses to the desired table size.

The registers of the address generation logic are accessed at DSP I/O locations 4 and 5. The ROM page and mask size register DSP I/O (location 4) bits are defined for the different table sizes as follows:

Bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A 8	A20	A19	A18	A17	A16	0	0	0
A15	A14	A13	A12	A11	A10	A9	A21	A20	A19	A18	A17	A16	0	0	1
A15	A14	A13	A12	A11	A10	A22	A21	A20	A19	A18	A17	A16	0	1	0
A15	A14	A13	A12	A11	A23	A22	A21	A 20	A19	A18	A17	A16	0	1	1
A15	A14	A13	A12	0	A23	A22	A21	A20	A19	A18	A17	A16	1	0	0
A15	A14	A13	0	0	A23	A22	A21	A20	A19	A18	A17	A16	1	0	1
A15	A14	0	0	0	A23	A22	A21	A20	A19	A18	A17	A16	1	1	0
0	0	0	0	0	A23	A22	A21	A20	A19	A18	A17	A16	1	1	1

The page/mask register supplies the table base address and the size of the extended memory table to be accessed, and the offset into the table is captured from the next value the DSP writes to any memory location from $6080 to $60BF. The number of significant bits of the table offset is determined by bits 2,1, and 0 of the mask register (above). For example, with table size set to 256 (mask bits = 000) only the lower 8 bits of the memory store are used, the upper 8 bits being ignored. After this memory store, there is a propagation delay through the SC1800X internal logic to the address outputs (maximum 50ns), and the address access time of the external extended memory (typically 200ns). The DSP may do other processing while waiting for this access to complete, and then read or write the extended memory by accessing DSP I/O port location 5. When the DSP accesses this port, the $\overline{\text{XROE}}$ pin goes low within 12ns to enable the extended memory access. If the extended memory output enable time is greater than 20ns, an external bus transceiver will be required. The direction control pin on this transceiver may be connected to $\overline{\text{XRWR}}$, which goes low to signal an extended memory write cycle.

The width of the extended memory being accessed is controlled by the XR16BIT input, when it is low the memory is read as 8 bit and placed in the high byte of the DSP 16 bit word with the lower byte zeroed. When this input is high, the extended memory is enabled as 16 bit wide, and the lower byte is not zeroed.

DAC SERIAL CONVERTER

This is a 16 bit latch loaded from DSP memory by direct memory access. At the beginning of each half sample period this value is transferred to a 16 bit shift register and then shifted out to an external stereo serial 16 bit DAC (left channel, then right channel). Data is sent on DACDATA MSB first, shifting on the falling edge of DACCLK (the external DAC used must clock data in on the rising edge of DACCLK). The data does not begin shifting out until 8 cycles after the beginning of a transfer cycle (8-bit clock cycles after a falling word-clock edge), so each channel transfer takes 24 DACCLK cycles (a stereo sample is output every 48 cycles). Note that since this is a stereo system, DMA transfers are required at twice the sample rate; this means that the DSP software should not use a repeat instruction (which disables DMA) for longer than this time less a safety factor.

Example:

sample rate = 44.1kHz

this means that the transfer rate = 88.2kHz

time between transfers = 1/transfer rate = 11.3µs

maximum repeat time = 50% of 11.3µs = 5.67µs or 60 cycles at 10.584MHz

Timing specifications

Skew of DACDATA change from DACCLK negative edge50ns max

Stereo sample rate 44.1kHz max (DACCLK = 2.1168MHz)

ADC SERIAL CONVERTER

This is an 8 or 16 bit (16 bit when the ADC16BIT input is high) shift register which reads data from an external ADC. After the shift register is completely full, the data is transferred to a 8 or 16 bit latch, and written into DSP memory by direct memory access. The stereo sample rate is the same as the DAC rate, set by the clock generation circuitry. ADC transfers occur in the same DMA cycle as the DAC transfers, and to the same memory location—basically a read-modify-write cycle. Left channel data is stored in even memory locations, right channel in odd locations. Monophonic inputs may be converted and stored at up to 88.2kHz by connecting both left and right channel ADC to the same input. In 8 bit transfer mode, the data is stored in the high byte of the DSP memory location and the lower byte is zeroed.

Both left and right channel data is received on ADCDATA most significant bit first, and clocked in on the rising edge of ADCCLK. ADCCLK is a gated clock, there are 8 cycles per channel for 8 bit mode, and 16 cycles per channel in 16 bit mode. The ADCCLK burst start is delayed 4 cycles from the ADCL/R transition, and the time between ADCL/R transitions is 24 bit clock cycles.

Timing specifications

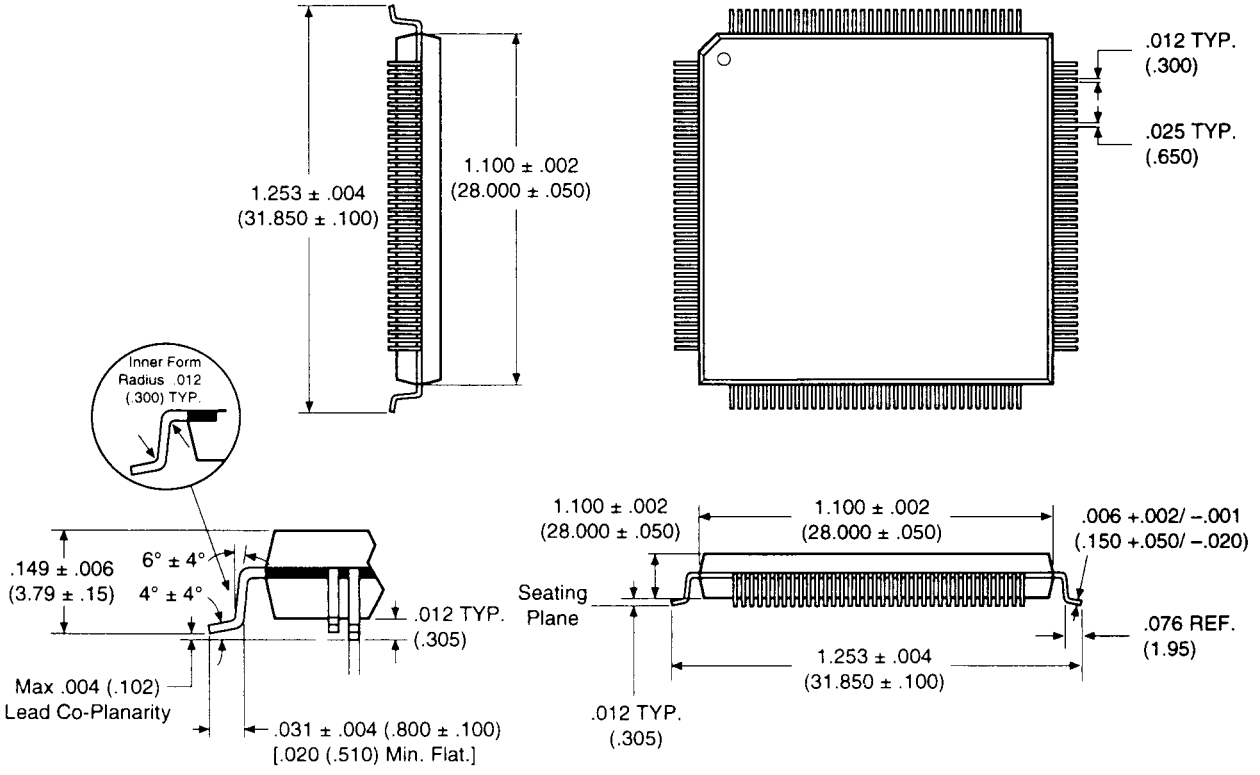
Setup time, ADCDATA to ADCCLK positive edge 25ns min

Hold time, ADCDATA from ADCCLK positive edge 25ns min

Stereo sample rate 44.1kHz max (DACCLK = 2.1168MHz)

PHYSICAL DIMENSIONS—INCHES (MILLIMETERS)

Package 144-Lead QFP (14mm)



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