NEC

MOS INTEGRATED CIRCUIT

μPD7759

ADPCM SPEECH SYNTHESIZER LSIs

The μPD7759 is an external ROM type speech synthesis LSI employing the waveform coding method. In addition to the ROM capability of up to 1 Mbit, the μPD7759 realizes the synthesis of speech sounds of any length by using the ADPCM data transferred from an external ROM.

As the synthesizing method, it adopts the ADPCM method and the PCM + waveform element method. The ADPCM method is suitable for synthesizing clear and natural speech sounds, and the PCM + waveform element method is for the synthesis of sound effects and melodies. And by using them together, the μPD7759 realizes the long-time synthesis of high-quality sounds.

Because of the short turn-around time of speech analysis, the μPD7759 can perform the quick system development using a PROM, or the evaluation of an on-chip ROM type of the μPD7755 family.

FEATURES

★ ● Synthesizing method : ADPCM, PCM + waveform element methods used together
● Sampling frequency : 5, 6 or 8 kHz
● Bit rate (speech) : 20 to 32 K bps
● Number of Messages : 256 (MAX.)
★ ● External speech data ROM

Parameters / Products	Speech data ROM (External)	Synthesizing time	
		Speech (ADPCM) Note1	Melodies & sound effects Note2 (PCM + waveform element)
μPD7759	1 Mbits	50 sec. (TYP.)	340 sec. (TYP.)

Note 1. The synthesizing time for the speech is the value for a 6 kHz sampling.

2. The synthesizing time for the melodies & sound effects is variable according to their tone.

● Speech output : Current sink type analog output, 9-bit D/A converter
● Host CPU interface : Compatible with a 4/8-bit CPU
● Standby mode : Pop-noise preventive circuit incorporated
● Supply voltage : 2.7 to 5.5 V
● CMOS technology

ORDERING INFORMATION

Part Number	Package	Quality grade
μPD7759C	40-pin plastic DIP (600 mil)	Standard
μPD7759GC-3BH	52-pin plastic QFP (□14 mm)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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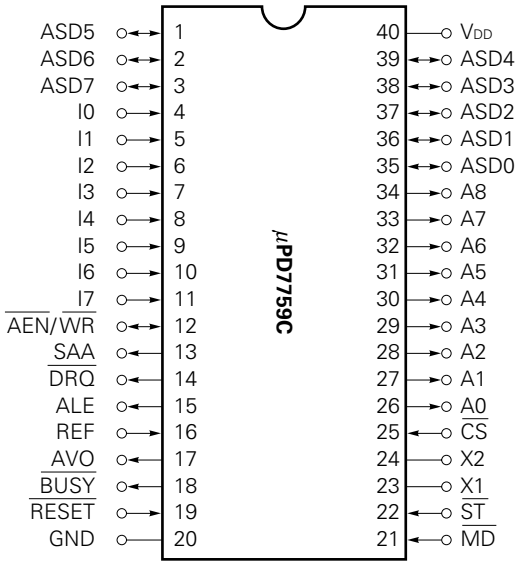
Date Published January 1993
Printed in Japan

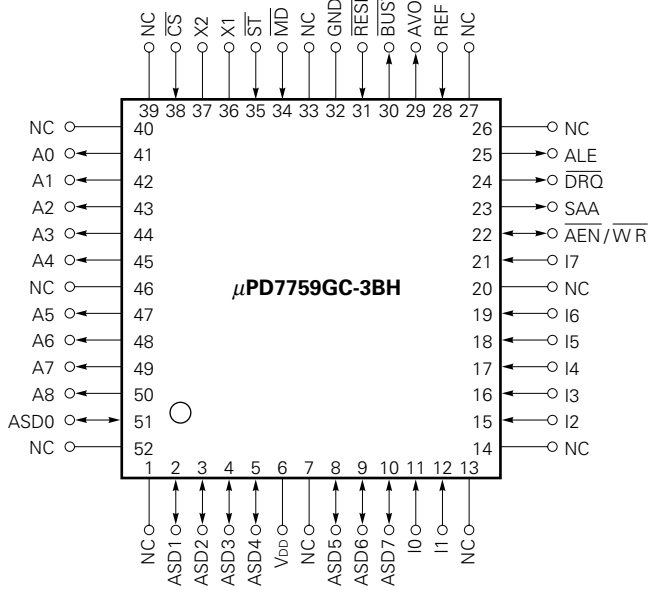
The mark ★ shows revised points.

PIN CONFIGURATION (Top View)

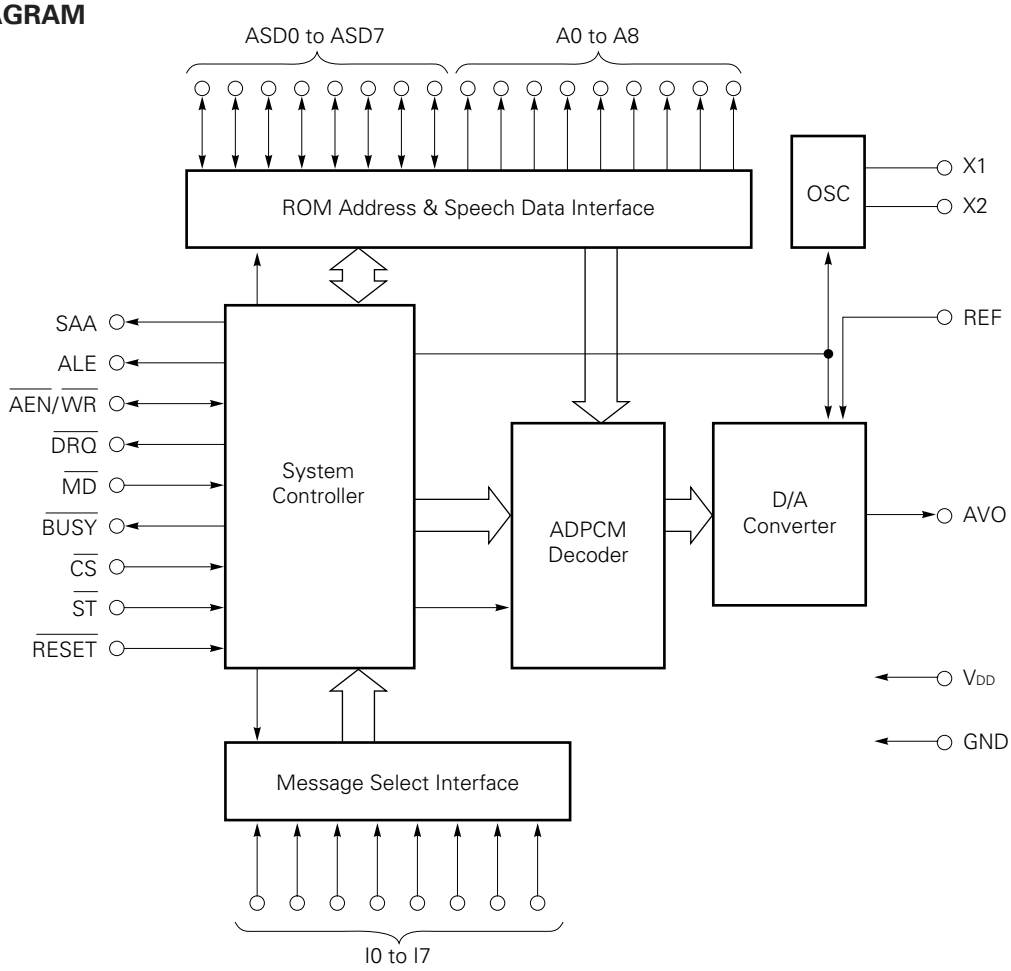
• **40-pin plastic DIP**



• **52-pin plastic QFP**



BLOCK DIAGRAM



1. PIN FUNCTIONS ★

1.1 COMMON FUNCTION TO ALL MODES

Pin (Abbre-viation)	52-pin QFP Pin No.	40-pin DIP Pin No.	I/O	Function
V_{DD}	6	40	—	Power supply (2.7 to 5.5 V)
$\overline{DRQ}$	24	14	Output	Speech synthesis data request.
REF	28	16	Input	D/A converter reference current input. The sink-load current input causes the output current of the D/A converter to change. The D/A converter reference current is passed to V_{DD} via a resistor. In standby mode, REF is set to high impedance.
AVO	29	17	Output	Analog speech signal output. AVO outputs a unipolar sink-load current. The output current is reduced to 0 when the μPD7759 is in the standby mode. The output current of the D/A converter from AVO is changed according to the input current from REF. Maximum output current of the D/A converter is approx. the 34 times the REF input current.
$\overline{BUSY}$	30	18	Output	Active-low $\overline{BUSY}$ signal output. When inputting $\overline{ST}$ signal, it outputs a low level signal. $\overline{MD}$, $\overline{ST}$ and $\overline{WR}$ are invalid while $\overline{BUSY}$ is low. In standby mode, $\overline{BUSY}$ is set to high impedance.
$\overline{RESET}$	31	19	Input	$\overline{Reset}$ input. In standby mode, $\overline{RESET}$ must be at low level more than 12 clock cycles after clock oscillation becomes stable. In operation mode, $\overline{RESET}$ must be at low level for 12 clock cycles (oscillation clock).
GND	32	20	—	Ground.
X1	36	23	—	Ceramic resonator connection for generating a clock signal. The 640 kHz ceramic resonator can be connected. In standby mode, the μPD7759 outputs a low-level to X1 and a high-level to X2.
X2	37	24	—	
NC	1, 7, 13, 14, 20, 26, 27, 33, 39, 40, 46, 52	—	—	No Connection

1.2 PIN FUNCTION FOR STAND ALONE MODE

Pin (Abbre-viation)	52-pin QFP Pin No.	40-pin DIP Pin No.	I/O	Function
I0 I1 I2 I3 I4 I5 I6 I7	11 12 15 16 17 18 19 21	4 5 6 7 8 9 10 11	Input	Message selection code input. The message selection code signals are positive logics. Ground the pins not used. These pins are connected to the internal latch circuit which latches I0 to I7 data at the rising edge of the $\overline{ST}$ input. In standby mode, these pins should be set high or low level. If they are biased at or near the typical CMOS threshold, the excess supply current is caused.
$\overline{AEN}$/$\overline{WR}$	22	12	Output/ Input	This signal is at low level while address signal is valid. Controls the latch circuit for the higher 8 bits of the external ROM address.
SAA	23	13	Output	Outputs high level when the start address of a message stored in the directory area of data memory, is being read out.
ALE	25	15	Output	Determines the timing that higher 8 bits of the external ROM address are externally latched. They must be latched at the falling edge of the signal.
$\overline{MD}$	34	21	Input	set at high-level.
$\overline{ST}$	35	22	Input	Start signal input. When $\overline{ST}$ goes low while $\overline{CS}$ is at low level, the μPD7759 starts synthesizing the message specified by I0 to I7. In standby mode, this signal resets the standby mode and starts speech synthesis.
$\overline{CS}$	38	25	Input	Chip select signal input. $\overline{ST}$ becomes valid when $\overline{CS}$ goes low.
A0 A1 A2 A3 A4 A5 A6 A7 A8	41 42 43 44 45 47 48 49 50	26 27 28 29 30 31 32 33 34	Output	Outputs the lower 9 bits of the external ROM address.
ASD0 ASD1 ASD2 ASD3 ASD4 ASD5 ASD6 ASD7	51 2 3 4 5 8 9 10	35 36 37 38 39 1 2 3	Input/ Output	(1) Outputs the higher 8 bits of external ROM address. (2) Inputs 8-bit speech synthesis data from the external ROM. These functions are executed from (1) to (2) on a time-shared basis.

1.3 PIN FUNCTION FOR SLAVE MODE

Pin (Abbre-viation)	52-pin QFP Pin No.	40-pin DIP Pin No.	I/O	Function
I0	11	4	Input	Invalid. Set at high or low level.
I1	12	5		
I2	15	6		
I3	16	7		
I4	17	8		
I5	18	9		
I6	19	10		
I7	21	11		
$\overline{AEN}$/$\overline{WR}$	22	12	Output/ Input	Inputs write strobe signal for a speech synthesis data.
SAA	23	13	Output	Invalid. Leave this pin open.
ALE	25	15	Output	Invalid. Leave this pin open.
$\overline{MD}$	34	21	Input	Slave mode selection input. Transition between two operation mode is not accepted during synthesis or in the standby mode.
$\overline{ST}$	35	22	Input	Invalid. Set at high level.
$\overline{CS}$	38	25	Input	Chip select signal input. $\overline{WR}$ becomes valid when $\overline{CS}$ goes low.
A0	41	26	Output	Invalid. Leave these pins open.
A1	42	27		
A2	43	28		
A3	44	29		
A4	45	30		
A5	47	31		
A6	48	32		
A7	49	33		
A8	50	34		
ASD0	51	35	Input	Input speech synthesis data from an external source.
ASD1	2	36		
ASD2	3	37		
ASD3	4	38		
ASD4	5	39		
ASD5	8	1		
ASD6	9	2		
ASD7	10	3		

2. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Parameters	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.3 to + 7.0	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_o		–0.3 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–40 to +125	°C
Operating temperature	T_{opt}		–10 to +70	°C

RECOMMENDED OPERATING CONDITIONS

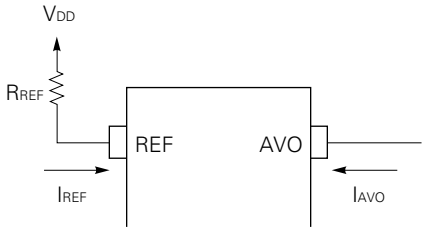
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.7		5.5	V
High-level input voltage	V_{IH1}	Applied to I0 to I7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Applied to ASD0 to ASD7, V_{DD} = 5 V ± 10 %	2.2		V_{DD}	V
Low-level input voltage	V_{IL1}	Applied to I0 to I7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$	0		0.3 V_{DD}	V
	V_{IL2}	Applied to ASD0 to ASD7, V_{DD} = 5 V ± 10 %	0		0.8	V
Clock frequency	f_{OSC}		630	640	650	kHz

Remark AC timing test voltage
$V_{IL} = V_{OL} = 0.3\ V_{DD}$
$V_{IH} = V_{OH} = 0.7\ V_{DD}$

DC CHARACTERISTICS (Ta = –10 to +70 °C, V_{DD} = 2.7 to 5.5 V, f_{OSC} = 640 kHz)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = –100 μA		V_{DD} –0.5		V
Low-level output voltage	V_{OL}	V_{DD} = 5 V ± 10 %, I_{OL} = 1.6 mA			0.4	V
Input leak current	$\lvert I_{LI} \rvert$	I_0 to I_7, $\overline{ST}$, $\overline{CS}$, $\overline{WR}$, ASD0 to ASD7, $\overline{MD}$			3	μA
Output leak current	$\lvert I_{LO} \rvert$	$\overline{BUSY}$, A0 to A8			3	μA
Supply current	I_{DD}	(Stand alone, slave mode) V_{DD} = 5 V			10	mA
		(Standby mode) V_{DD} = 5 V			20	μA
		(Stand alone, slave mode) 2.7 V ≦ V_{DD} ≦ 3.5 V			1	mA
		(Standby mode) 2.7 V ≦ V_{DD} ≦ 3.5 V			10	μA
Reference input current [Note]	I_{REF}	V_{DD} = 2.7 V, R_{REF} = 0 Ω	140	250	440	μA
		V_{DD} = 5.5 V, R_{REF} = 0 Ω	500	760	1200	μA
		V_{DD} = 2.7 V, R_{REF} = 50 kΩ	21	30	39	μA
		V_{DD} = 5.5 V, R_{REF} = 50 kΩ	68	78	88	μA
D/A converter output current	I_{AVO}	2.7 V ≦ V_{DD} ≦ 5.5 V V_{AVO} = 2.0 V, D/A input: 1 FFH	32 I_{REF}	34 I_{REF}	36 I_{REF}	μA
D/A converter output leak current	$\lvert I_{LD} \rvert$	0 V ≦ V_{AVO} ≦ V_{DD} in the standby mode			5	μA

Note Measuring circuit



★ **AC CHARACTERISTICS (Ta = –10 to +70 °C, V_{DD} = 2.7 to 5.5 V, f_{OSC} = 640 kHz)**

TIMING REQUIREMENTS (common to all modes)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{BUSY}$ rise time	t_{r1}	C_L = 150 pF, V_{DD} = 5 V ± 10 %			800	ns
	t_{r2}	C_L = 150 pF, V_{DD} = 2.7 to 5.5 V			2	μs
$\overline{BUSY}$ fall time	t_{f1}	C_L = 150 pF, V_{DD} = 5 V ± 10 %			800	ns
	t_{f2}	C_L = 150 pF, V_{DD} = 2.7 to 5.5 V			2	μs
$\overline{BUSY}$ output stop time	t_{RB}	from $\overline{RESET}$ ↓			9.5	μs

2.1 STAND ALONE MODE

(1) TIMING REQUIREMENTS

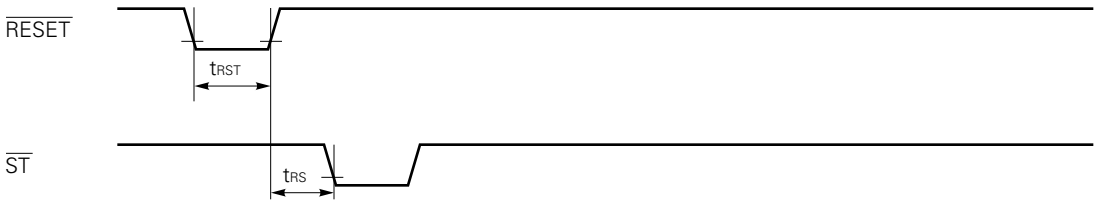
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{RESET}$ pulse width	t_{RST}		18.5			μs
$\overline{CS}$ set up time	t_{CS}	for $\overline{ST}$ ↓	0			ns
$\overline{CS}$ hold time	t_{SC}	from $\overline{ST}$ ↑	0			ns
★ $\overline{ST}$ set up time	t_{RS}	In operation mode, from $\overline{RESET}$ ↑	200			μs
		In standby mode, from $\overline{RESET}$ ↑	1.6			ms
$\overline{ST}$ pulse width	t_{CC}	2.7 V ≦ V_{DD} ≦ 5.5 V	2			μs
		4.5 V ≦ V_{DD} ≦ 5.5 V	350			ns
Message select code set up time	t_{DW}	2.7 V ≦ V_{DD} ≦ 5.5 V, from $\overline{ST}$ ↑	5			μs
		4.5 V ≦ V_{DD} ≦ 5.5 V, from $\overline{ST}$ ↑	350			ns
Message select code hold time	t_{WD}	from $\overline{ST}$ ↑	0			ns
Speech data set up time	t_{DR}	for $\overline{DRQ}$ ↓	2		7.5	μs
Speech data hold time	t_{RDH}	from $\overline{DRQ}$ ↑			1.25	μs

(2) SWITCHING CHARACTERISTICS

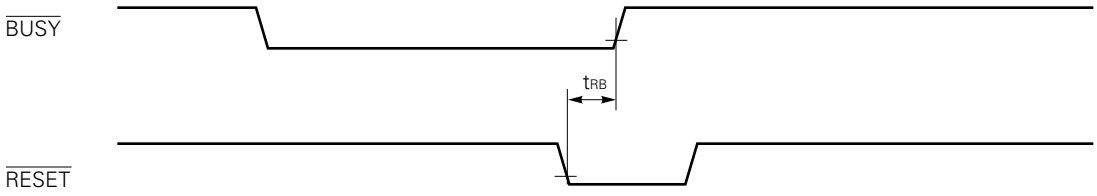
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{BUSY}}$ output delay	t_{SBO}	In operation mode, from $\overline{\text{ST}}$ ↓		6.25	10	μs
Speech output delay	t_{SSO}	In operation mode, from $\overline{\text{BUSY}}$ ↓		2.1	2.2	ms
$\overline{\text{BUSY}}$ hold time	t_{BD}	from synthesis			15	μs
ALE pulse width	t_{LL}			3.13		μs
Higher address set up time	t_{AL}	for ALE ↓		3.13		μs
	t_{AE}	for $\overline{\text{AEN}}$ ↓		0		μs
Higher address hold time	t_{LA}	from ALE ↓		3.13		μs
	t_{EA}	from $\overline{\text{AEN}}$ ↑		0		μs
$\overline{\text{AEN}}$ pulse width	t_{AEN}			14.1		μs
$\overline{\text{DRQ}}$ output delay	t_{LC}	from ALE ↓		3.13		μs
Higher address pulse width	t_{AC}			6.25		μs
$\overline{\text{DRQ}}$ pulse width	t_{DCC}			7.81		μs
ROM read cycle time	t_{MRO}			37.5		μs

TIMING CHART (at reset)

(1)

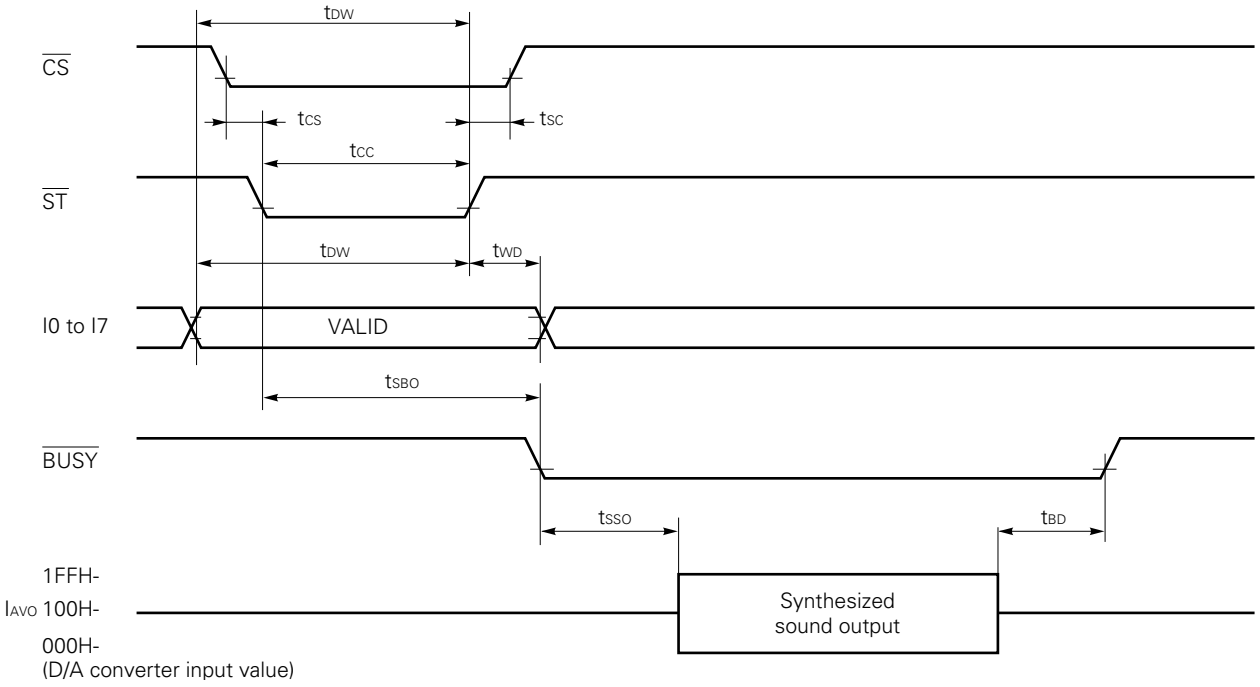


(2)

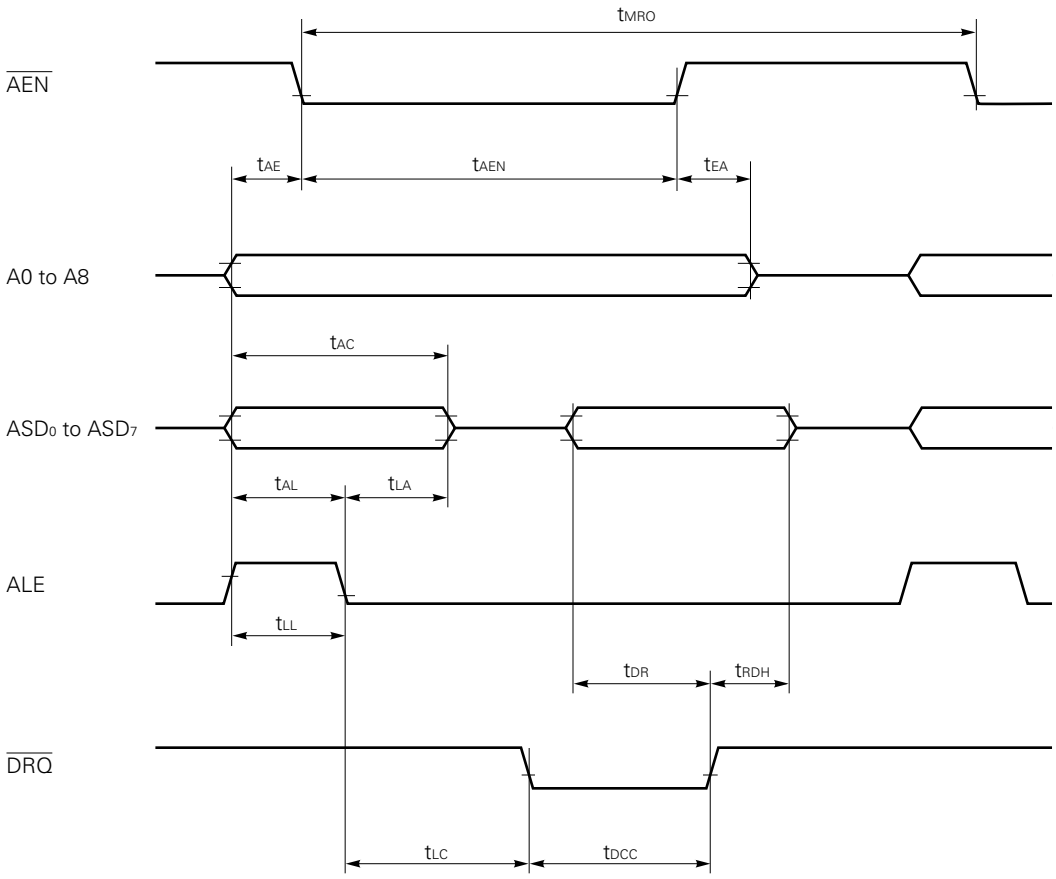


TIMING CHART (Stand alone mode)

(1) CONTROL



(2) MEMORY ACCESS



2.2 SLAVE MODE

(1) TIMING REQUIREMENTS

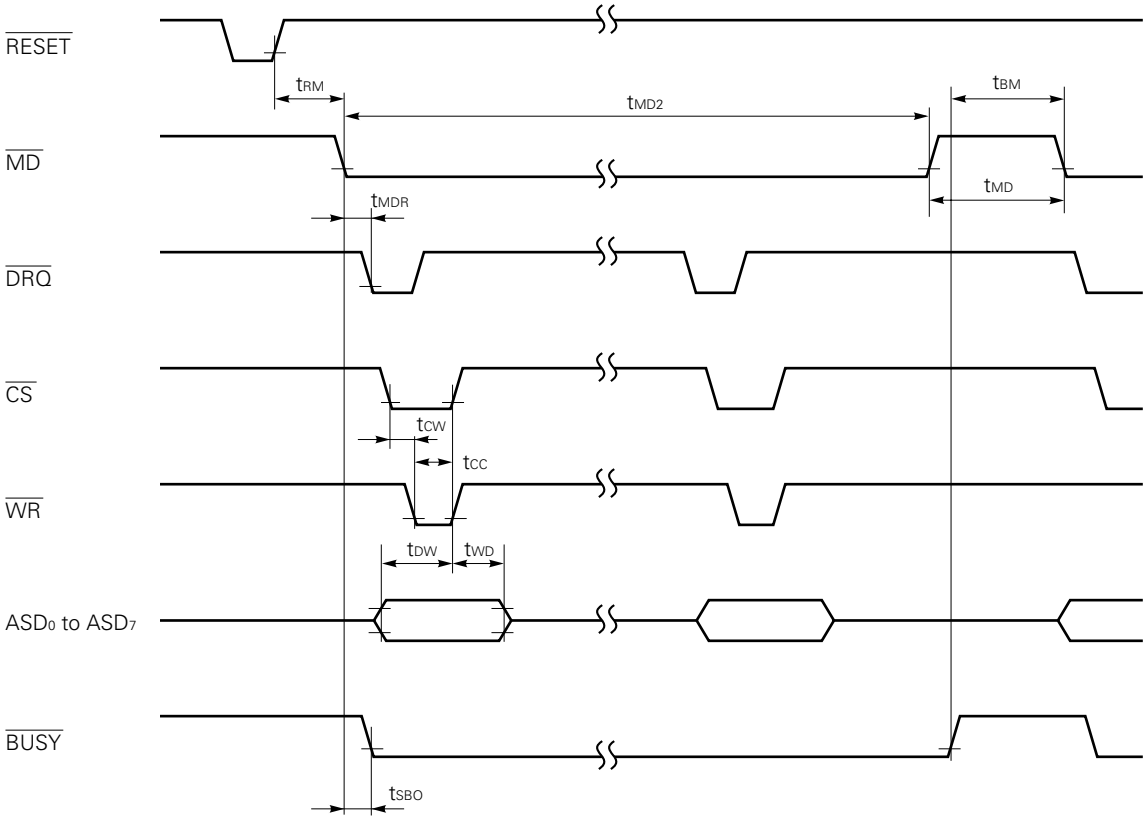
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{MD}$ set up time	t_{RM}	from $\overline{RESET}$ ↑	200			μs	
	t_{BM}	from $\overline{BUSY}$ ↑	0			ns	★
	t_{MD}	from $\overline{MD}$ ↑	6.2			μs	
$\overline{MD}$ pulse width	t_{MD2}		6.2			μs	
Speech data set up time	t_{DW}	for $\overline{WR}$ ↑, 5 V ± 10 %	350			ns	
Speech data hold time	t_{WD}	from $\overline{WR}$ ↑, 5 V ± 10 %	0			ns	
$\overline{WR}$ input stop time	t_{WR}	from $\overline{DRQ}$ ↓			31.7	μs	
$\overline{WR}$ pulse width	t_{CC}	5 V ± 10 %	350			ns	
$\overline{CS}$ set up time	t_{CW}	for $\overline{WR}$ ↓	0			ns	
$\overline{CS}$ hold time	t_{WC}	from $\overline{WR}$ ↑	0			ns	

(2) SWITCHING CHARACTERISTICS

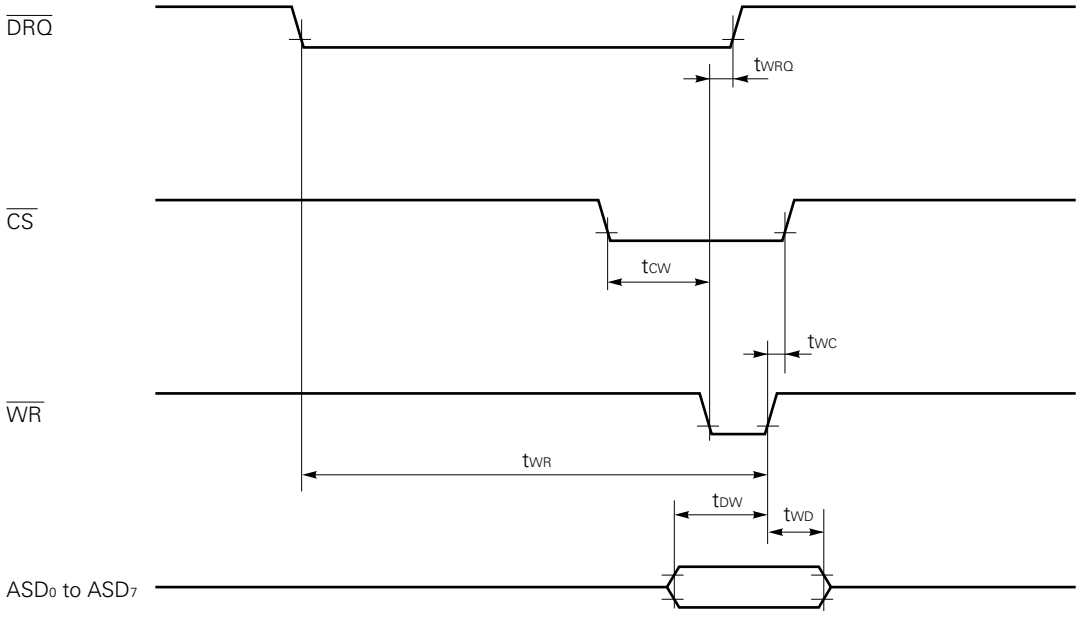
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{BUSY}$ output delay	t_{SBO}	from $\overline{MD}$ ↓			9.5	μs	
$\overline{DRQ}$ output delay	t_{MDR}	In operation mode, from $\overline{MD}$ ↓	50		70	μs	★
		In standby mode, after $\overline{RESET}$ input, from $\overline{MD}$ ↓	50		50000		
$\overline{DRQ}$ output stop time	t_{WRQ}	from $\overline{WR}$ ↓			3	μs	

TIMING CHART (Slave mode)

(1) CONTROL



(2) DATA TRANSFER



2.3 STANDBY MODE

(1) TIMING REQUIREMENTS

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby escape signal L*[Note] pulse width	t_{AW}	V_{DD} = 5 V ± 10 %	350			ns

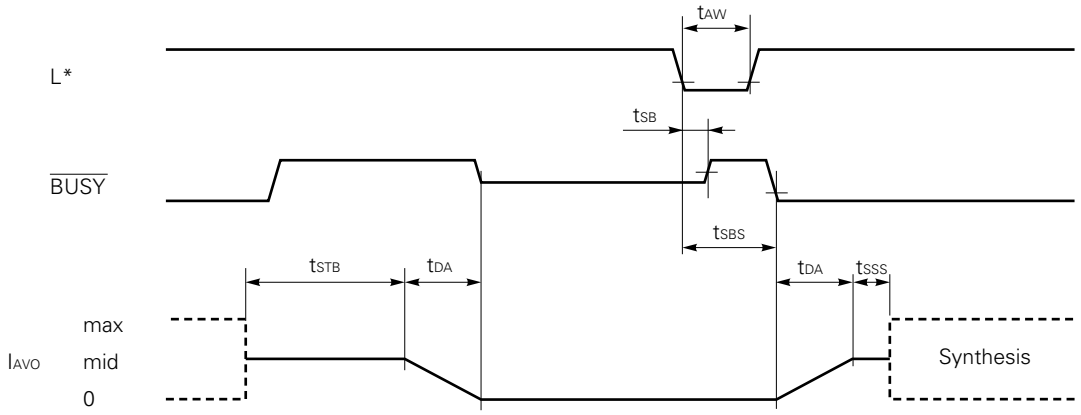
(2) SWITCHING CHARACTERISTICS

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation mode hold time	t_{STB}	after synthesis		2.9	3	s
D/A converter activate /inactivate time	t_{DA}			46.5	47	ms
$\overline{BUSY}$ set up time	t_{SB}	from L* ↓		6.25	10	μs
Synthesis start time	t_{SSS}	after D/A converter activation		2.1	2.2	ms
$\overline{BUSY}$ output delay	t_{SBS}	In standby mode, oscillation start time is included.		4	80	ms

Note L*: Signal to release standby mode.

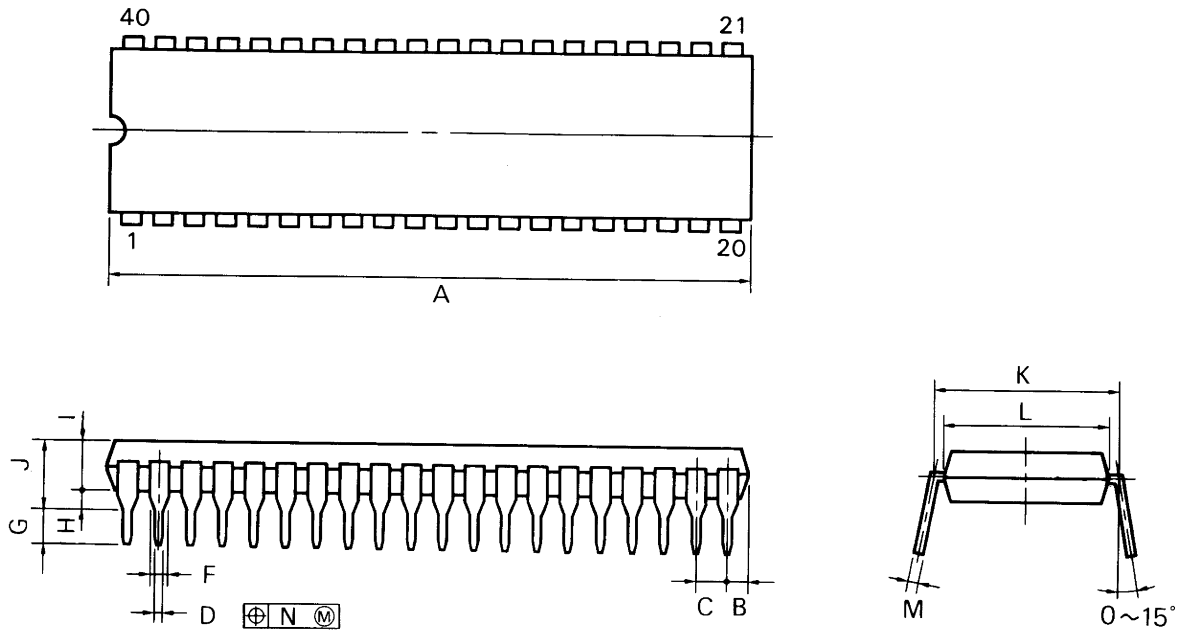
$$= \begin{cases} \overline{CS} \wedge \overline{ST} : \text{When operation mode is stand alone mode.} \\ \overline{CS} \wedge \overline{WR} : \text{When operation mode is slave mode} \end{cases}$$

TIMING CHART (Standby mode)



3. PACKAGE DRAWINGS

40PIN PLASTIC DIP (600 mil)



P40C-100-600A

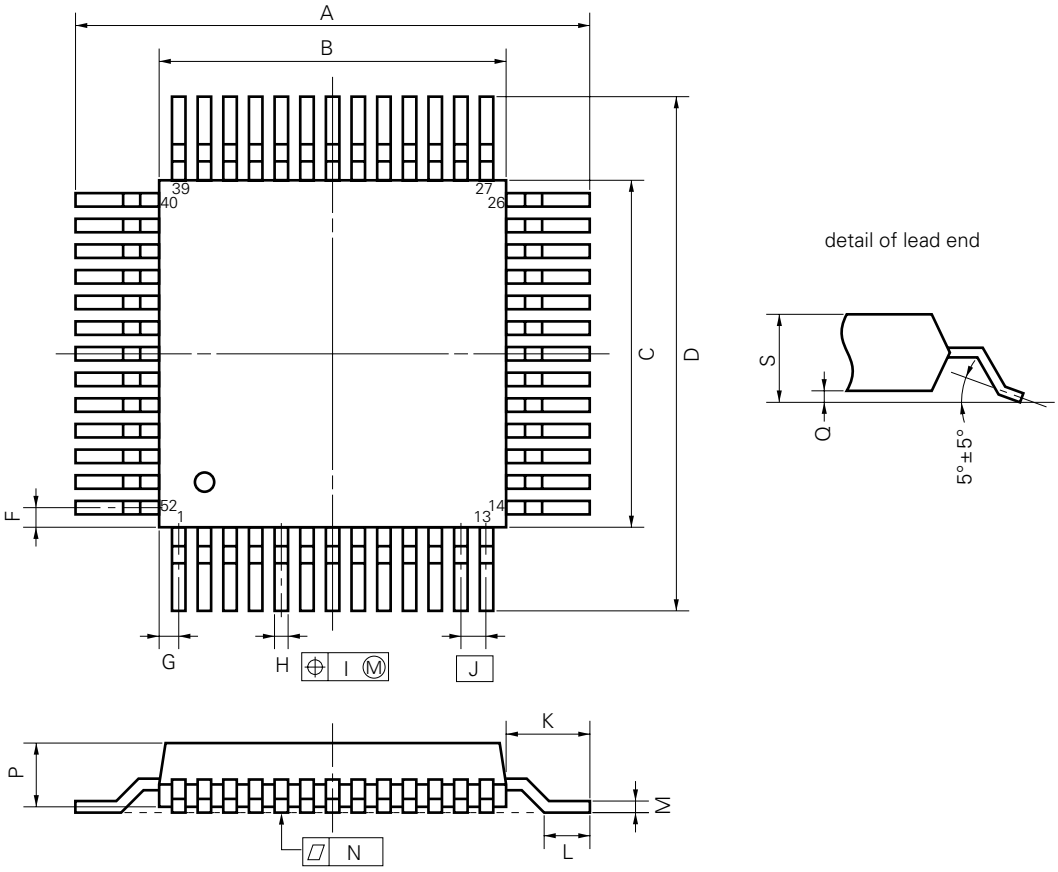
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.6^{+0.3}$	$0.142^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

★ 52 PIN PLASTIC QFP (□14)



P52GC-100-3B6,3BH-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

4. RECOMMENDED SOLDERING CONDITIONS ★

The following conditions (see tables below) must be met when soldering the μPD7759. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"** (IEI-1207).

○ **TYPE OF SURFACE MOUNT DEVICE**

μPD7759GC-3BH:52-pin plastic QFP (□14 mm)

Soldering Process	Soldering Conditions	Symbol
Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Temperature of pre-heat: 120 °C or below (Plastic surface temperature), Number of flow process: 1	WS60-00-1
Infrared Ray Reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1	IR30-00-1
VPS	Peak package's temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1	VP15-00-1
Partial Heating Method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one side of the device)	—

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

○ **TYPE OF THROUGH HOLE DEVICE**

μPD7759C:40-pin plastic DIP (600mil)

Soldering Process	Soldering Conditions
Wave Soldering (only lead part)	Solder Temperature: 260 °C or below Flow time: 10 seconds or below
Partial Heating Method	Terminal temperature: 260 °C or below Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.

The μPD7759 has the following user's manual as a separate volume.
Please use it for reference.

- μPD7755 family User's Manual: IEU-1218

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