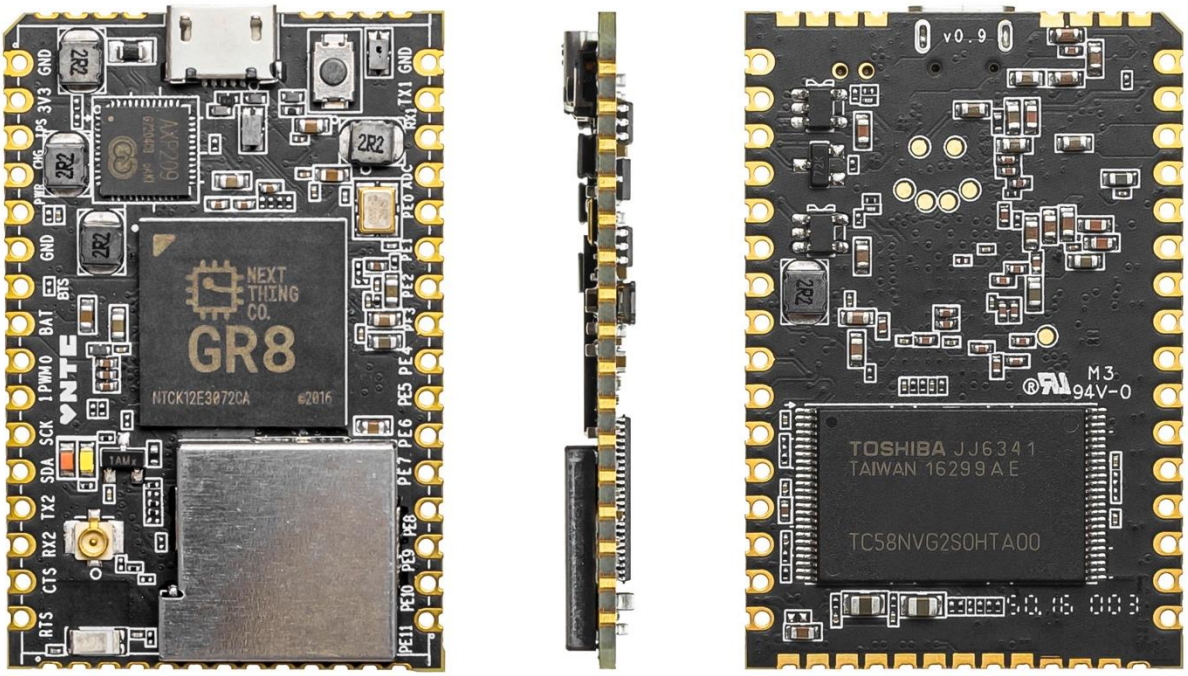

C.H.I.P. Pro Datasheet

Version 1.02
2017-03-06

Revision History

Revision	Date	Description
v0.1	Oct. 09, 2016	Initial Internal Release
v1.0	Oct. 11, 2016	Initial Public Release
V1.01	Dec. 20, 2016	Updated PCB Footprint and Pinout Map
V1.02	Mar. 06, 2017	Updated Pinout Map, Mech. Drawing, Photos, Removed erroneous application diagram

Declaration

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About This Documentation

From the desk of Gustavo Huber

When Dave, Thomas, and I started Next Thing Co. in 2013, it was with a simple goal: we wanted to create things that would inspire creativity, and help people chase their own ideas of what needed to exist.

We considered this goal both in terms of how economically accessible we could make our products (they had to be $99 or less), as well as how much "pain" we could remove from the design process for others (they had to be open source and well-documented).

Our first attempt was a software-defined camera named OTTO, built around an off-the-shelf embedded module. But early in development, we knew that our end-goals were at risk. The $39 module made it impossible to ship product priced under $99. It lacked Mainline Linux support, a reliable tool-chain, documentation and functional drivers making software development a cat-and-mouse game of bug tracking. But thanks to lots of long days, and some good friends both in Shenzhen and back home in Oakland, we built and shipped out 500 OTTOs -- a serious feat.

Almost exactly a year later, we shipped out the first of what is now over 100,000 C.H.I.P.s delivered worldwide. At $9, C.H.I.P. was the fruition of our vision from a year prior: accessible, powerful technology, available to everyone for hobby, education, or products. In so many words, we were building the tools that we wished we'd had before.

The reaction was (and continues to be) astounding! Tweets and emails come from far and wide to tell us about impossible projects banged together in an afternoon, classrooms full of proud 10-year-old game developers who had never before written a line of code, and seasoned engineers brought back to memories of discovering their passion on a Commodore 64, 40 years prior. Yet, just as building OTTO showed us the tools we were missing, building C.H.I.P has taught us what it takes to scale production to keep up with [even unprecedented] demand.

So it is with great pleasure that I invite you to explore, without non-disclosure agreements or any other obstructive formalities, this datasheet for C.H.I.P. Pro: the newest addition to the Next Thing Co. family.

Thanks to the experience and support from our friends at Allwinner and Nanya, C.H.I.P. Pro is built from the ground up for clean and reliable design. From in-package DDR3 DRAM in the GR8 SiP (which allows us to buy known-good-die DRAM rather than market components), to keeping the onboard NAND, Bluetooth, Wifi, and power management that made C.H.I.P. so useful, C.H.I.P. Pro takes care of all the nuts and bolts, letting you get to the fun parts faster.

With Next Thing Co. and the thriving Chipster community from bbs.nextthing.co at your side, we can't wait to see what you'll do with C.H.I.P. Pro!

/Gustavo
Co-founder, Hardware Guy

1. Overview

At Next Thing Co., we work to make it easy to integrate computer hardware in products. C.H.I.P. Pro is powered by GR8, a system-in-package (SiP) that was designed by Next Thing Co. GR8 features a 1GHz Allwinner R8 ARM Cortex-A8 processor, Mali400 GPU, and 256MB of Nanya DDR3 DRAM in a 14mm x 14mm FBGA package.

C.H.I.P. Pro is a system-on-module (SoM) that has 512MB of high-speed NAND storage flashed with our GadgetOS. It can be powered by USB or battery, intelligently managed by the AXP209 power management unit.

The module offers all the popular interfaces you'd expect. With two UARTs, a Two Wire Interface, a parallel camera interface, SPI, two PWM channels, USB 2.0 OTG port, and a USB 2.0 Host port, C.H.I.P. Pro is packed full of I/O expandability. Comprehensive audio handling includes a built-in 24-bit ADC/DAC for analog audio, One Wire Audio digital out, and I2S digital audio for interfacing with professional audio codecs.

C.H.I.P. Pro is CE, IC, and FCC part 15 modularly certified, making integration into end products easy. The on-board Realtek 8723DS combination module provides compliant Wi-Fi B/G/N and Bluetooth 4.2 Low-Energy connectivity. A software controlled antenna path selects between the on-board chip antenna or a uFL antenna connector where several pre-certified antennas can be added to boost wireless transmit and receive range.

Rated to operate from 2.9V-6V input in environments ranging between 0 and 70 degrees Celsius and measures 45 mm x 30 mm.

C.H.I.P. Pro is $16 in any quantity and includes custom factory flashing via Next Thing Co.'s Gadget software tools for orders of 1000 or more. The minimum order quantity for C.H.I.P. Pro is one.

We can't wait to see how you'll integrate C.H.I.P Pro in to your next product.

1.1. Applications

- Physical Computing
- Voice Recognition
- Smart "Clapper"
- Animated GIF Camera
- Smart Consumer Devices
- Portable Audio Devices
- Cyber Dog Robot Toys

2. Features

2.1. CPU

- ARM Cortex™-A8
- ARMv7 Instruction set plus Thumb-2 Instruction Set
- 32KB Instruction Cache and 32KB Data Cache
- 256KB L2 Cache
- NEON™ SIMD Extensions
- Jazelle RCT Acceleration

2.2. GPU

- Mali400
- Supports Open GL ES 1.1/ 2.0 and Open VG 1.1

2.3. Memory

Boot ROM
- On-chip Boot ROM
- Supports NAND Flash, SPI NOR Flash, SD Card and USB OTG

NANYA DDR3 SDRAM
- In-package 256MB 16-bit DDR3 memory

NAND Flash
- 512MB SLC NAND

SD/MMC
- One SD/MMC Host Controllers (SMHC)
- Compatible with eMMC v4.4, SD Physical Layer Specification v2.0, SDIO Card Specification v2.0
- 1-/4-/8-bit bus width
- Supports block size of 1 to 65535 bytes
- Dedicated DMA for fast and uninterrupted data transfer

2.4. System Peripherals

CCM – Clock Control Module
- Seven PLLs driven by a main external Oscillator and an on-chip RC Oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

DMA – Direct Memory Access
- Eight channels Normal DMA (NDMA) and eight channels Dedicated DMA (DDMA)
- Supports memory-to-memory, memory-to-peripheral, peripheral-to-memory data transfer types
- Transfer data width of 8/16/32-bits
- Programmable DMA burst size

PWM – Pulse Width Modulation
- Two outputs
- Supports continuous and pulse waveforms
- 0% to 100% adjustable duty cycle
- Up to 24 MHz output frequency

Asynchronous Timer
- Six Asynchronous Timers with interrupt-based operation
- A watchdog timer to generate reset signal or interrupt
- Two 33-bit Audio/Video Sync (AVS) counter to synchronize video and audio
- One 64-bit counter

Synchronous Timer
- Two Synchronous Timers with interrupt-based operation

Interrupt Controller
- Normal interrupt requests (nIRQ) and fast interrupt requests (FIQ)
- Supports 96 interrupt sources
- Four level priority controller
- External interrupt can be triggered according to edge or level-sensitivity

LRADC – Low Resolution Analog-to-Digital Converter
- Analog-to-Digital Converter with 6-bit resolution suitable for multi-button input
- Supports multiple button press detection
- Supports single, normal and continuous work mode
- Sampling frequency up to 250 Hz

Crypto Engine
- Supports AES, DES, 3DES, SHA-1, MD5
- Supports ECB, CBC modes for AES/DES/3DES
- 128-bit, 192-bit and 256-bit key size for AES
- 160-bit hardware Pseudo Random Number Generator (PRNG) with a 175 bit seed

2.5. Video Engine

Video Decoding
- Supports multi-format video decoding of VP6/8, AVS, H.264, H.263, and MPEG-1/2/4
- Up to 1080p@30fps resolution

Video Encoding
- Supports encoding in H.264 MP format
- Up to 720p@30fps resolution

2.6. Display Subsystem

Display Processing
- Four moveable and size-adjustable layers
- Multi-format image input
- Image enhancement processor
- Alpha blending /anti-flicker
- Hardware cursor
- Output color correction (luminance/hue/saturation)

2.7. Image Input

- Supports 8-bit CMOS sensor parallel interface
- Supports BT656 interface
- Maximum still capture resolution on parallel interface up to 5M
- Maximum video capture resolution on parallel interface up to 1080p@30fps
- Pixel clock up to 150MHz

2.8. Audio Subsystem

Audio Codec – Audio Compression / Decompression Module
- On-chip 24-bit DAC for playback and ADC for recording
- Supports analog/digital volume control
- Supports 44.1 kHz, 48 kHz, 96 kHz, and 192 kHz sample rates
- Stereo microphone input
- Stereo headphone amplifier

I2S/PCM – Inter-IC Sound / Pulse Code Modulation
- Selectable I2S or PCM on shared pins
- Full-duplex synchronous serial interface
- Configurable as a master or a slave
- Audio data resolutions of 16, 20, 24
- I2S Audio data sample rate from 8 kHz to 192 kHz
- Left Justified or Right Justified I2S
- PCM supports 8-bit or 16-bit linear, 8-bit u-law, or 8-bit A-law companding sample format
- One 128x24−bits FIFO for data transmit and one 64x24−bits FIFO for data receive
- Programmable FIFO thresholds

OWA - One Wire Audio
- IEC-60958 transmitter functionality
- Channel status insertion
- Hardware parity generation
- One 32×24bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds

2.9. External Peripherals

USB – Universal Serial Bus
- One USB 2.0 OTG controller
  - Complies with USB 2.0 Specification
  - Supports High-Speed (HS,480 Mbit/s), Full-Speed (FS,12 Mbit/s) and Low-Speed (LS,1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Up to 10 user-configurable endpoints in device mode
- One USB Host controller
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) mode

TWI - Two Wire Interface
- One TWI (Two-Wire Interface) controller
- Supports Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s)
- Configurable as a master or a slave
- Capable of 10-bit addressing

UART - Universal Asynchronous Receiver/Transmitter
- Two UART controllers
  - UART0 with 2 wires
  - UART1 with 4 wires
- Compatible with industry-standard 16550 UARTs
- Support for word length from 5 to 8 bits, an optional parity bit, and 1, 1.5 or 2 stop bits
- Programmable parity (even, odd and no parity)

SPI – Serial Peripheral Interface
- One SPI controller with one Chip Select signal
- Full-duplex synchronous serial interface
- Configurable as a master or a slave
- Configurable Polarity, phase and clock frequency

2.10. **Power System**

AXP209 Power Management Unit

- Intelligent Power Select (IPS) allows for three separate inputs: Vbus-USB (VBUS), Charge-In (CHG-IN), and Battery (BAT)
- Li-Po Battery Charging up to 1.8A with configurable current limiting, and Fuel Gauge Functionality
- Integrated ON/OFF button configurable logic, interrupt and startup/shutdown sequencing
- Integrated battery temperature sensor circuit, alternately usable as 12-bit ADC

2x LY8088 Switching Regulators

- 1.3A 2.3V-6V Input, 1.5MHz Synchronous Step-Down Converter

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

The absolute maximum ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may cause damage to the device.

Table 3.1: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
$I_{I/O}$	In/Out Current for Input and Output		-40	40	mA
CHG-IN	Input Voltage for Charge-In		-0.3	11	V
BAT	Input Voltage for Battery-in		-0.3	4.2	V
VBus	Input Voltage for USB-VBus		-0.3	11	V
T_{STG}	Storage Temperature		-30	125	°C
T_A	Ambient Operating Temperature (1)		0	70	°C
P_D	PMU Internal Power Dissipation		-	2100	mW
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM) (2)	-4000	4000	V
		Charged Device Model(CDM) (3)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin (4)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin (5)		Pass		

(1) Limited by operating temperature minimum of WiFi+BT Module, other components tested to -20C.
(2) Test method: JEDEC JS-001-2014(Class-3A). JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) Test method: JEDEC JS-002-2014(Class-C2A). JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(4) Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.
(5) Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

3.2. Recommended Operating Conditions

All C.H.I.P Pro modules are used under the operating conditions contained in Table 5-2.

Table 3.2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
CHG-IN	Input Voltage for Charge-In	3.8	5~5.5	6.3	V
BAT	Input Voltage for Battery-In	3.0	3.8	4.2±0.5%	V
VBus	Input Voltage for VBus	3.8	5~5.5	6.3	V
I_{OUT}	PMU V_{OUT} Current available before loading BAT (1)	500	900	2500	mA

(1) Programmable limit set in AXP209 PMU allows for safe attachment to USB 2.0, USB 3.0, or high-current CHG-IN sources.

3.3. DC Electrical Characteristics

Table 5.3 summarizes the DC electrical characteristics of C.H.I.P Pro.

Table 3.3: DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	50	100	150	KΩ
R_{PD}	Input Pull-down Resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

3.4. Power Consumption Summary

At the time of this document's publication we are still testing the C.H.I.P. Pro power consumption. For the latest document version, please see our git repository at https://github.com/NextThingCo/CHIP_Pro-Hardware

3.5. Oscillator Electrical Characteristics

C.H.I.P. Pro contains a single 24.000MHz oscillator.

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN. Table 5-4 lists the 24.000MHz crystal specifications.

Table 3.4: 24MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25 °C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum Change Over Temperature Range	-50	-	+50	ppm
P_{ON}	Drive Level	-	-	300	uW
C_L	Equivalent Load Capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	-	25	-	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	-	-	pF

C_{SHUT}	Shunt Capacitance	5	6.5	7.5	pF
R_{BIAS}	Internal Bias Resistor	0.4	0.5	0.6	MΩ

3.6. **Power Up/Down and Reset Specifications**

C.H.I.P. Pro only requires that you apply voltage within the acceptable range to any or all of the AXP209's Intelligent Power Select inputs. Power up and power down sequence requirements for the GR8 SiP are handled by the on-board Power System provided by the AXP209 PMU and companion switching regulators.

For more details in specific system submodule power up/down timing and requirements, please review the GR8 SiP documentation and AXP209 datasheet available at https://github.com/NextThingCo/CHIP_Pro-Hardware

4. Block Diagram

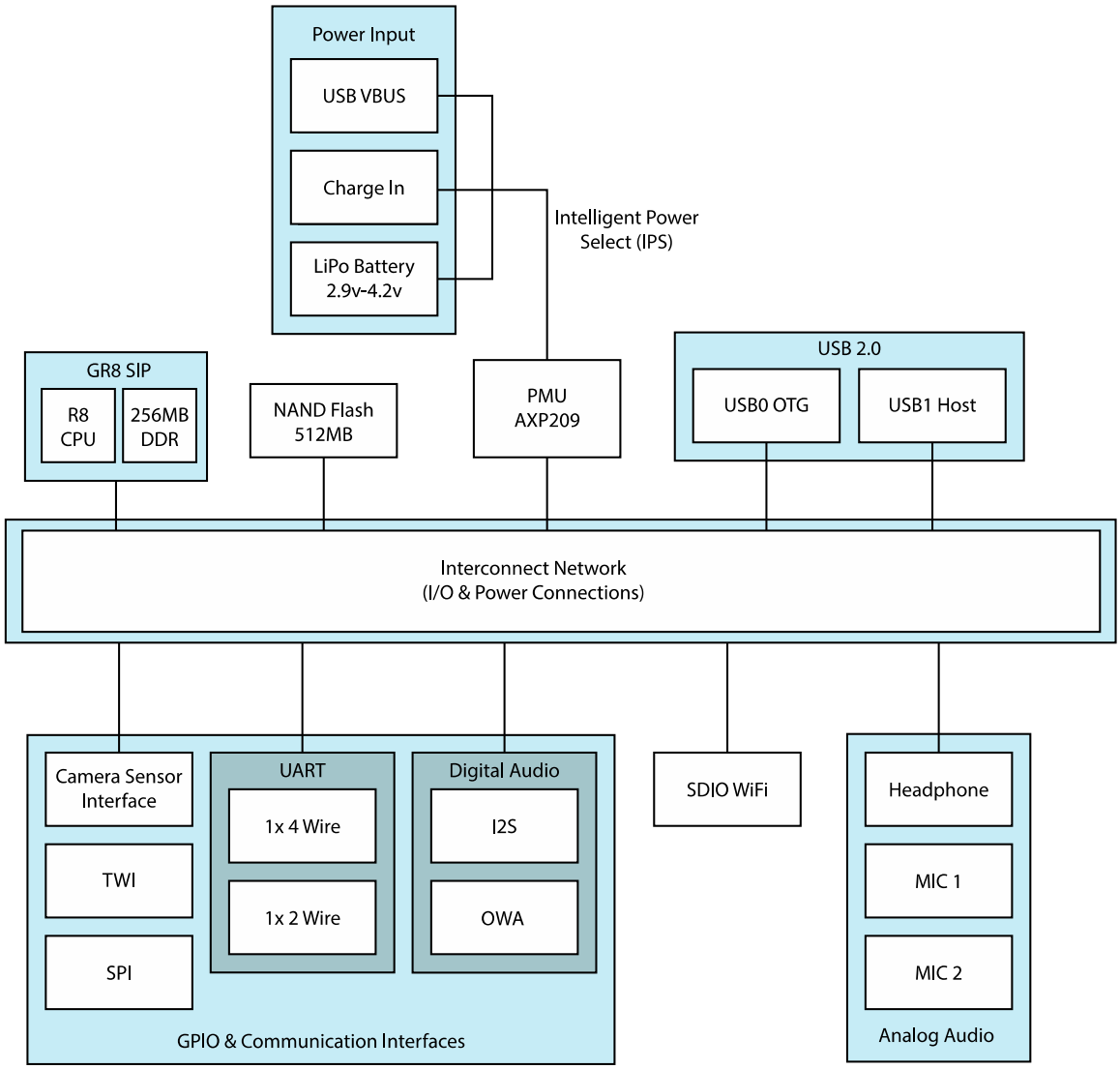


Figure 3.1:. C.H.I.P. Pro Block Diagram

5. Pin Description

5.1. Pin Characteristics

Table 4-1 lists the characteristics of C.H.I.P Pro pins from the following aspects: Pin Number, Pin Name, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

1) **Pin Number:** Through-holes + Castellated Edges
2) **Pin Name**: Names of signals multiplexed on each pin No.
3) **Type:** Signal direction
   I : Input
   O: Output
   I/O: Input / Output
   A: Analog
   AIO: Analog Input / Output
   OD: Open Drain
   P: Power
   G: Ground
4) **Pin Reset State:** The state of the terminal at reset (power up)
   Z: High-impedance
5) **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister
   Pull up and pull down resistor can be enabled or disabled via software.
6) **Buffer Strength:** Drive strength of the associated output buffer.

Table 5-5. Pin Characteristics

Pin #	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
PORT B						
9	PB2	GPIO	I/O	Z	NO PULL	20
21	PB5	GPIO	I/O	Z	NO PULL	20
22	PB6	GPIO	I/O	Z	NO PULL	20
23	PB7	GPIO	I/O	Z	NO PULL	20
24	PB8	GPIO	I/O	Z	NO PULL	20
25	PB9	GPIO	I/O	Z	NO PULL	20
12	PB15	GPIO	I/O	Z	NO PULL	20
11	PB16	GPIO	I/O	Z	NO PULL	20
PORT D						
13	PD2	GPIO	I/O	Z	NO PULL	20
14	PD3	GPIO	I/O	Z	NO PULL	20
15	PD4	GPIO	I/O	Z	NO PULL	20
16	PD5	GPIO	I/O	Z	NO PULL	20
PORT E						

Pin #	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
41	PE0	GPIO	I/O	Z	NO PULL	20
40	PE1	GPIO	I/O	Z	NO PULL	20
39	PE2	GPIO	I/O	Z	NO PULL	20
38	PE3	GPIO	I/O	Z	NO PULL	20
37	PE4	GPIO	I/O	Z	NO PULL	20
36	PE5	GPIO	I/O	Z	NO PULL	20
35	PE6	GPIO	I/O	Z	NO PULL	20
34	PE7	GPIO	I/O	Z	NO PULL	20
33	PE8	GPIO	I/O	Z	NO PULL	20
32	PE9	GPIO	I/O	Z	NO PULL	20
31	PE10	GPIO	I/O	Z	NO PULL	20
30	PE11	GPIO	I/O	Z	NO PULL	20
PORT G						
44	PG3	GPIO	I/O	Z	NO PULL	20
43	PG4	GPIO	I/O	Z	NO PULL	20
USB						
52	USB0-DM	-	A I/O	-	-	-
51	USB0-DP	-	A I/O	-	-	-
48	USB1-DM	-	A I/O	-	-	-
47	USB1-DP	-	A I/O	-	-	-
50	VCC-USB	-	P	-	-	-
Audio Codec						
26	AGND	-	G	-	-	-
19	HPCOM	-	AO	-	-	-
18	HPL	-	AO	-	-	-
20	HPR	-	AO	-	-	-
27	MICIN1	-	AI	-	-	-
28	MICIN2	-	AI	-	-	-
29	VMIC	-	AO	-	-	-
LRADC						
42	LRADC0	-	AI	-	-	-
Power						
2	VDD-3V3	-	P	-	-	-
4	CHG-IN	-	P	-	-	-
8	BAT	-	P	-	-	-
GND						
1, 6, 17, 45, 46, 49, 53	GND	-	G	-	-	-

5.2. GPIO Multiplexing Functions

The following table provides a description of the GR8 GPIO multiplexing functions.

Table 5.6**: Multiplexing Functions**

Port	Multi0	Multi1	Multi2	Multi3	Multi4	Multi5	Multi6
Port B							
PB2	Input	Output	PWM0				EINT16
PB5	Input	Output	I2S-MCLK				EINT19
PB6	Input	Output	I2S-BCLK				EINT20
PB7	Input	Output	I2S-LRCK				EINT21
PB8	Input	Output	I2S-DO				EINT22
PB9	Input	Output	I2S-DI				EINT23
PB15	Input	Output	TWI1-SCK				
PB16	Input	Output	TWI1-SDA				
Port D							
PD2	Input	Output	LCD-D2	UART2-TX			
PD3	Input	Output	LCD-D3	UART2-RX			
PD4	Input	Output	LCD-D4	UART2-CTS			
PD5	Input	Output	LCD-D5	UART2-RTS			
Port E							
PE0	Input			CSI-PCLK	SPI2-CS0		EINT14
PE1	Input			CSI-MCLK	SPI2-CLK		EINT15
PE2	Input			CSI-HSYNC	SPI2-MOSI		
PE3	Input	Output		CSI-VSYNC	SPI2-MISO		
PE4	Input	Output		CSI-D0	SDC2-D0		
PE5	Input	Output		CSI-D1	SDC2-D1		
PE6	Input	Output		CSI-D2	SDC2-D2		
PE7	Input	Output		CSI-D3	SDC2-D3		
PE8	Input	Output		CSI-D4	SDC2-CMD		
PE9	Input	Output		CSI-D5	SDC2-CLK		
PE10	Input	Output		CSI-D6	UART1-TX		
PE11	Input	Output		CSI-D7	UART1-RX		
Port G							
PG3	Input	Output	SDC1-CMD		UART1-TX		EINT3
PG4	Input	Output	SDC1-CLK		UART1-RX		EINT4
PG13	Input	Output		PWM1			EINT13

Note: PE0/PE1/PE2 are for input only in GPIO configuration.

5.3. Detailed Pin/Signal Description

Table 4.3 shows the detailed function of every pin/signal based on the different interface.

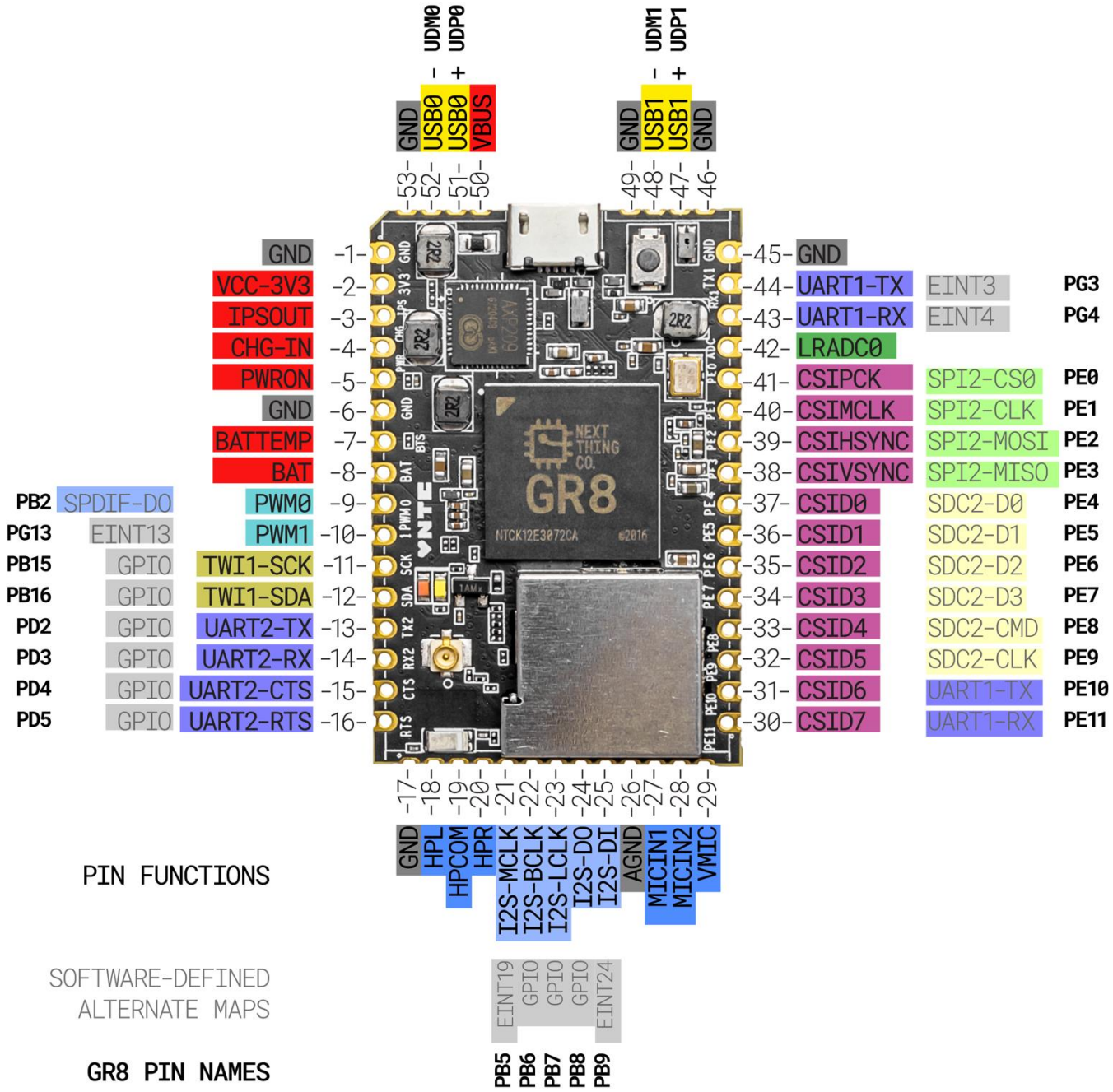
Table 4.7: Detailed Pin/Signal Description

Pin/Signal Name	Description	Type
TWI – Two Wire Interface		
TWI1-SCK	TWI1 Clock	I/O
TWI1-SDA	TWI1 Data/Address	I/O
PWM – Pulse Width Modulation		
PWM0	Pulse Width Module Channel0 Output	O
PWM1	Pulse Width Module Channel1 Output	O
I2S – Inter-IC Sound		
I2S-MCLK	I2S Master Clock	O
I2S-BCLK	I2S Bit Clock	I/O
I2S-LRCK	I2S Left/Right Channel Select Clock	I/O
I2S-DO	I2S Data Output	O
I2S-DI	I2S Data Input	I
OWA – One Wire Audio		
OWA-DO	OWA Data Output	O
SPI – Serial Peripheral Interface		
SPI2-CS0	SPI0 Chip Select Signal (active low)	I/O
SPI2-CLK	SPI0 Clock Signal	I/O
SPI2-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI2-MOSI	SPI0 Master Data Out, Slave Data In	I/O
UART – Universal Asynchronous Receiver/Transmitter		
UART1-TX	UART0 Data Transmit	O
UART1-RX	UART0 Data Receive	I
UART2-TX	UART1 Data Transmit	O
UART2-RX	UART1 Data Receive	I
UART2-CTS	UART1 Data Clear to Send	I
UART2-RTS	UART1 Data Request to Send	O
CSI – Camera Sensor Interface		
CSI-PCLK	CSI Pixel Clock	I
CSI-MCLK	CSI Master Clock	O
CSI-HSYNC	CSI Horizontal Sync	I
CSI-VSYNC	CSI Vertical Sync	I
CSI-Data[7:0]	CSI Data Bit	I
SD/MMC		
SDC2-D[3:0]	SDC2 Data Bit [3:0]	I/O

Pin/Signal Name	Description	Type
SDC2-CLK	SDC2 Clock	O
SDC2-CMD	SDC2 Command Signal	I/O
External Interrupt		
EINT[3,4,13,19,24]	External Interrupt Input	I
USB		
USB0-DM	USB0 D- Signal	A I/O
USB0-DP	USB0 D+ Signal	A I/O
USB1-DM	USB1 D- Signal	A I/O
USB1-DP	USB1 D+ Signal	A I/O
VCC-USB	USB Power Supply	P
Audio Codec		
AGND	Audio Codec Analog Ground	G
HPCOM	Headphone Common Reference Output	AO
HPL	Headphone Left Channel Output	AO
HPR	Headphone Right Channel Output	AO
MICIN1	Microphone Input	AI
MICIN2	Microphone Input	AI
VMIC	Bias Voltage Output for Main Microphone	AO
LRADC – Low Resolution Analog-to-Digital Converter		
LRADC0	ADC Input for Channel 0 for Multi-Button Input	AI

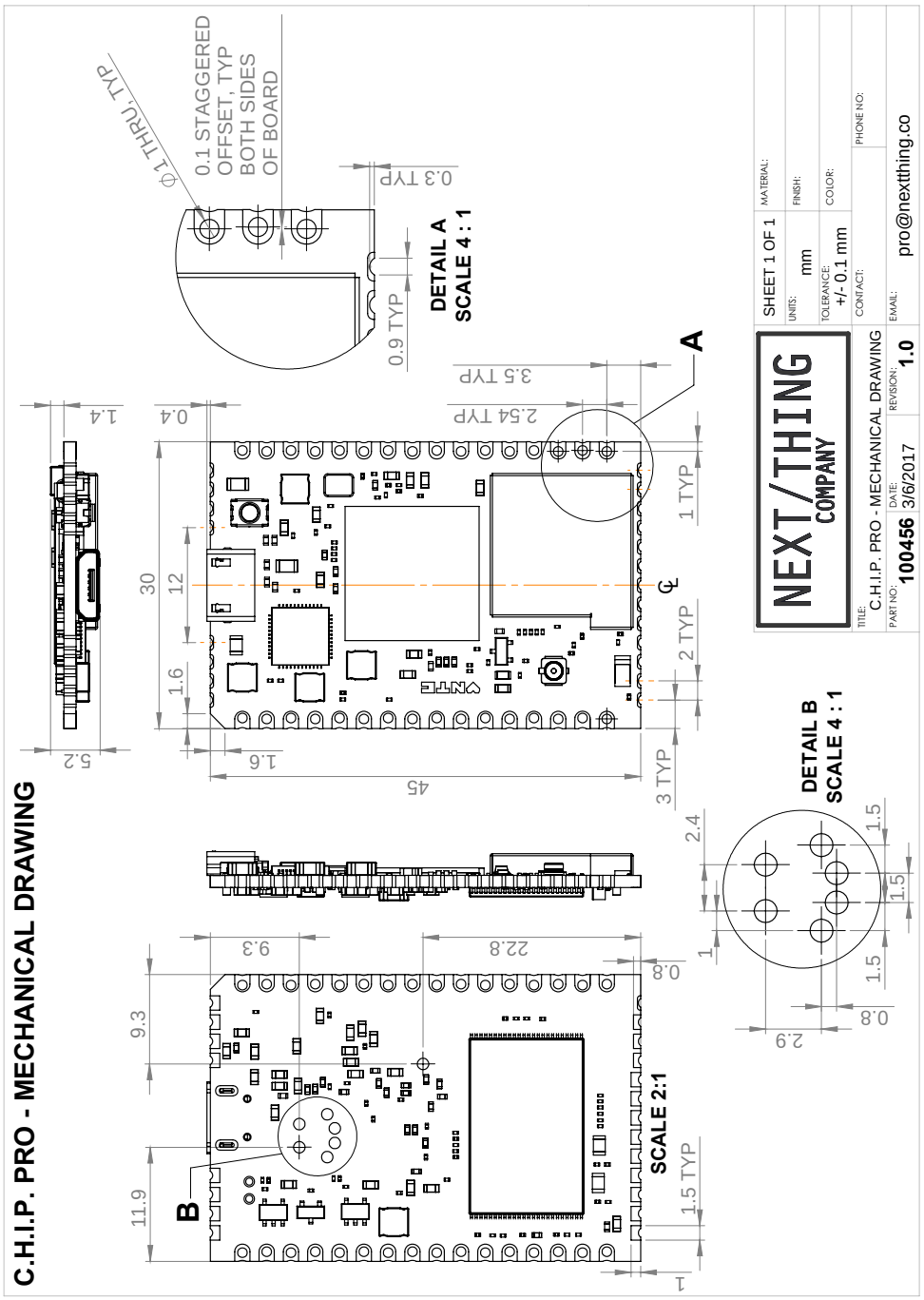
5.4. **Pinout Diagram**

The following pin map demonstrates the alternate pin mux configurations possible in a top view of the C.H.I.P. Pro.

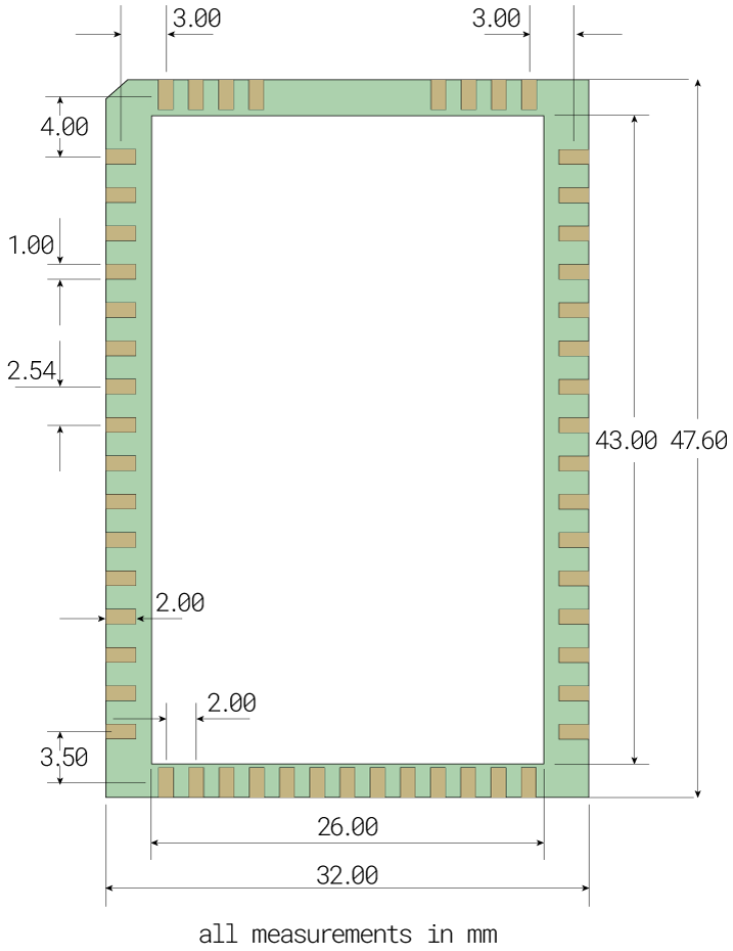


6. Mechanical and Packaging Information

The following diagram shows the package specification of C.H.I.P. PRO module including top, bottom, and side views.

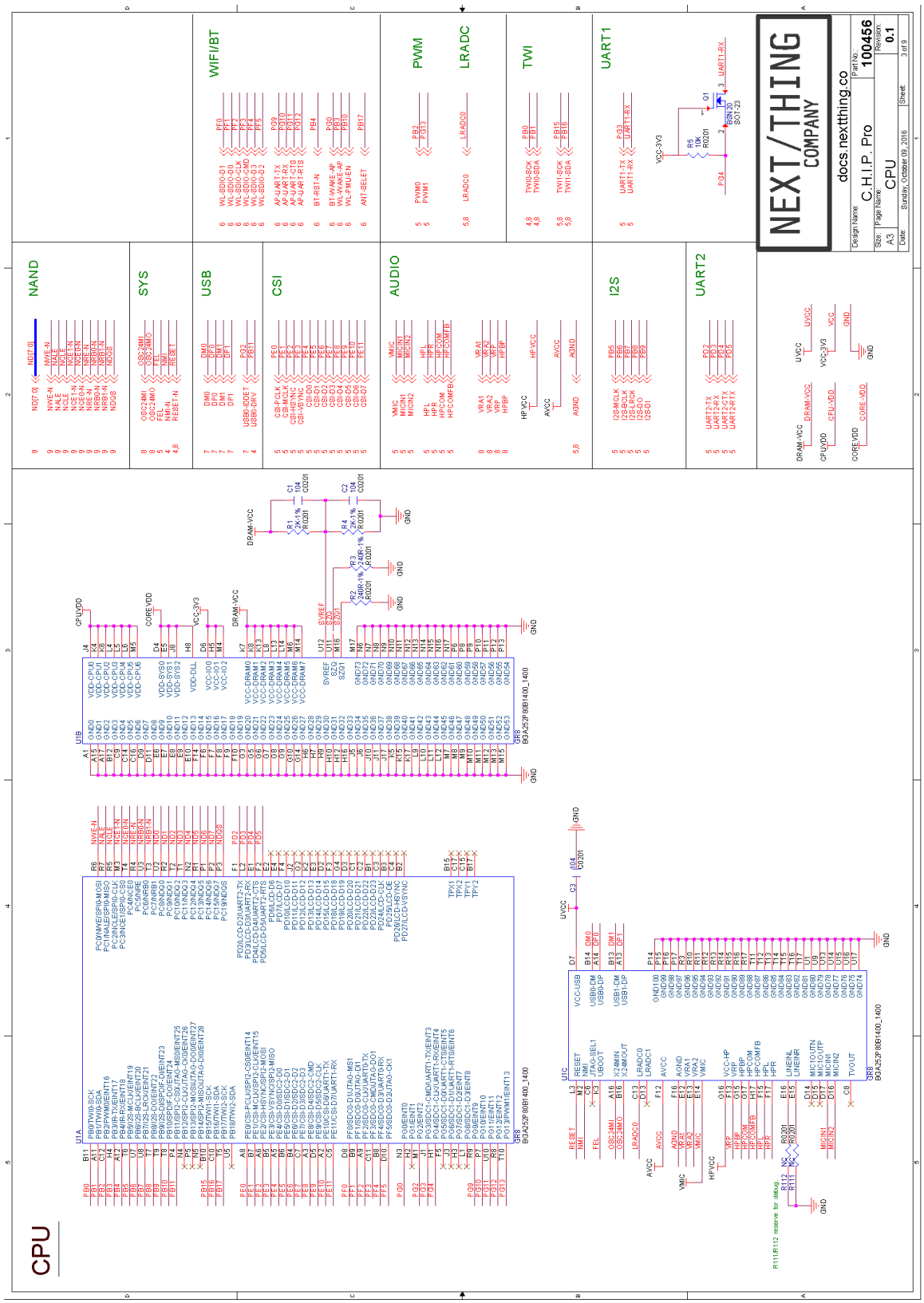


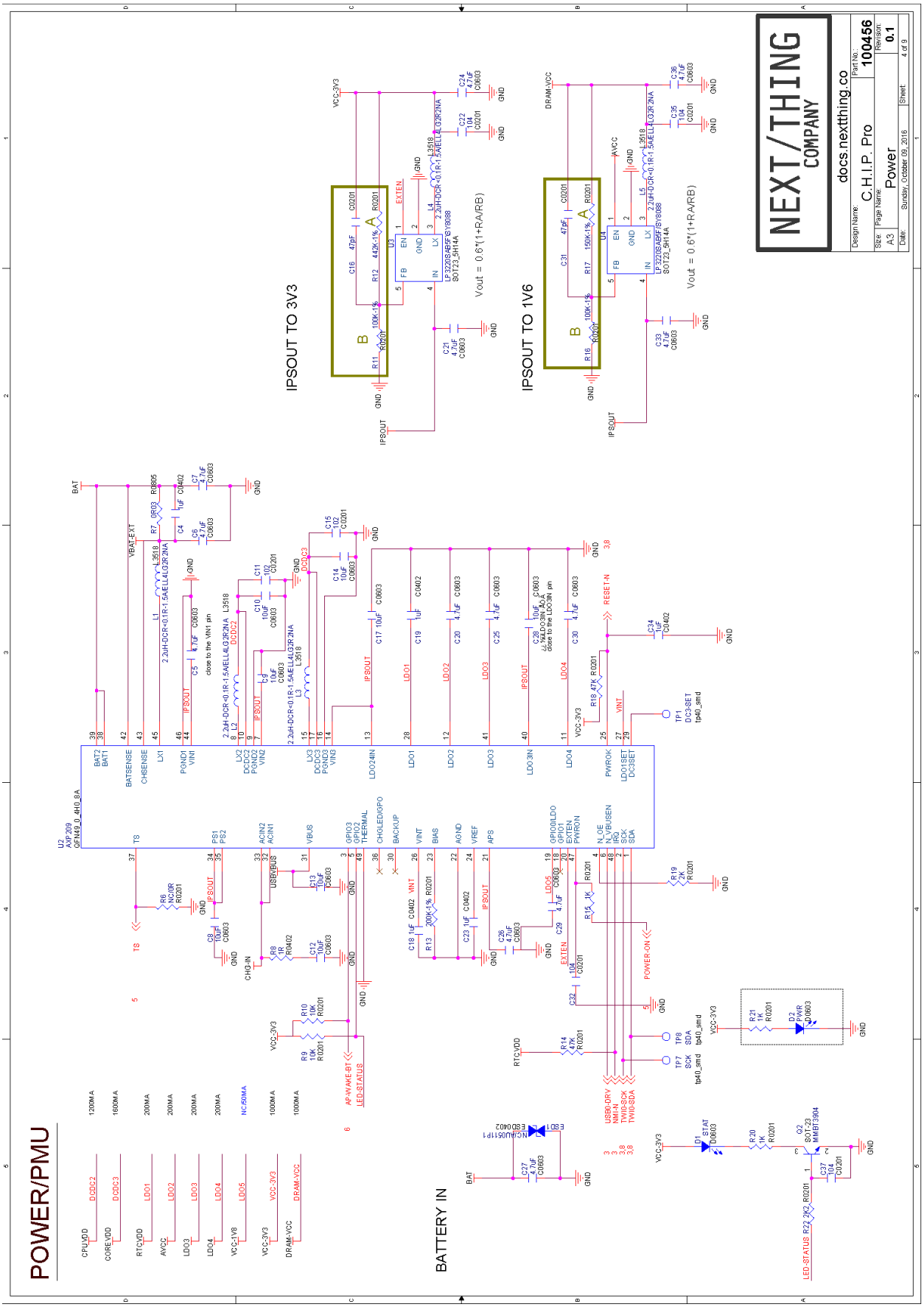
6.1. Recommended PCB Footprint

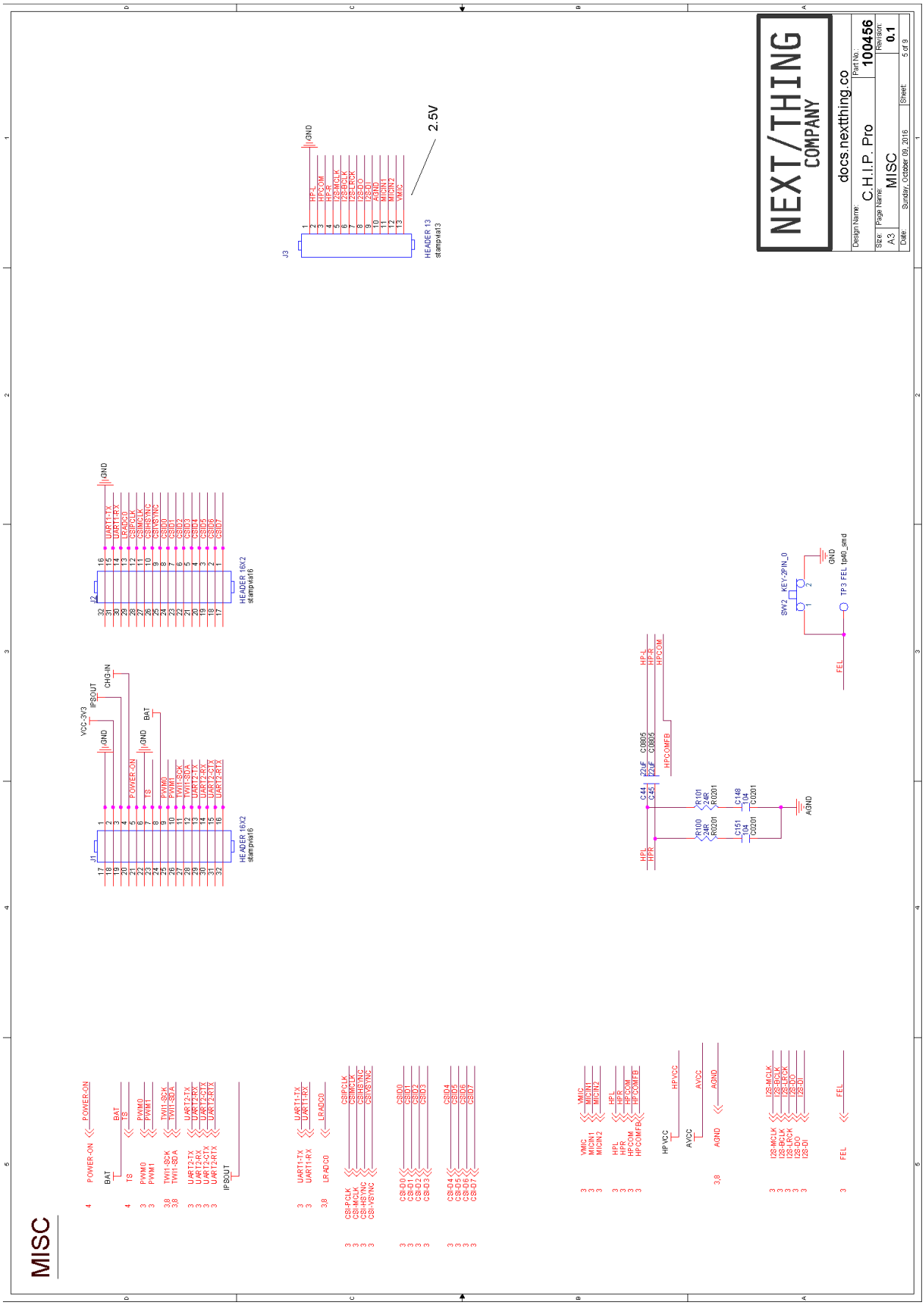


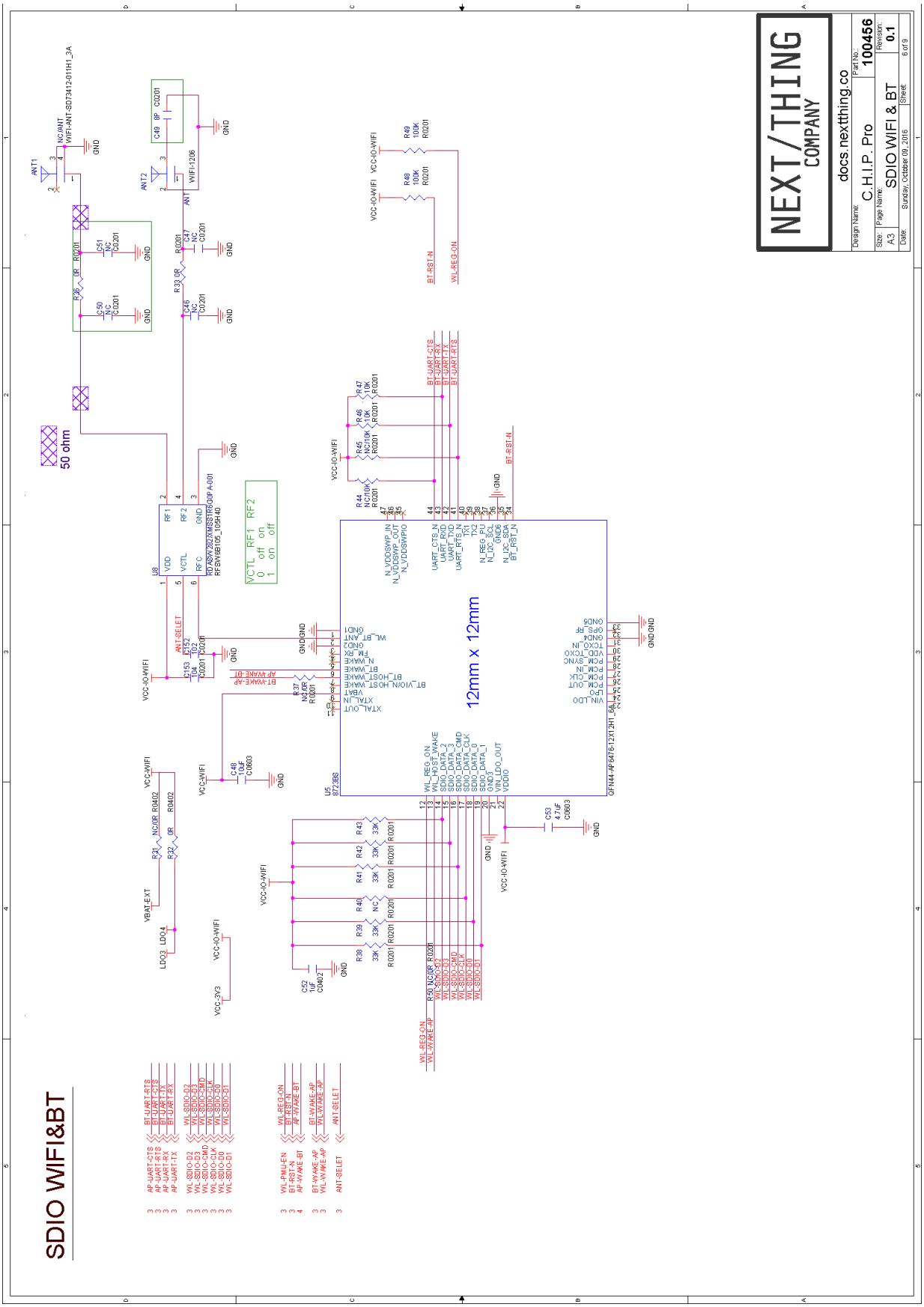
NOTE:
Part footprints for common EDA Software Packages are made available at https://github.com/NextThingCo/CHIP_Pro-Hardware

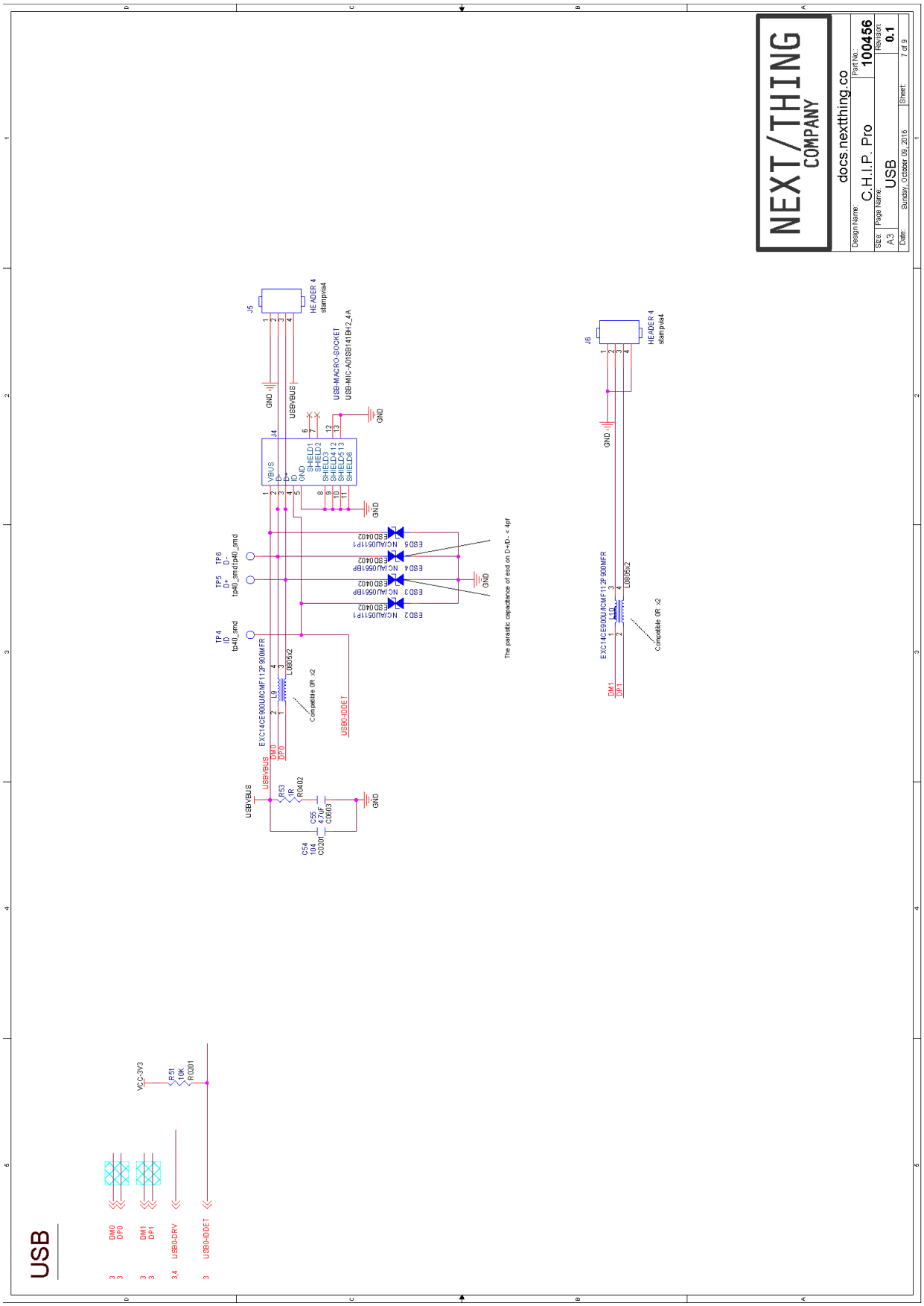
7. Schematic

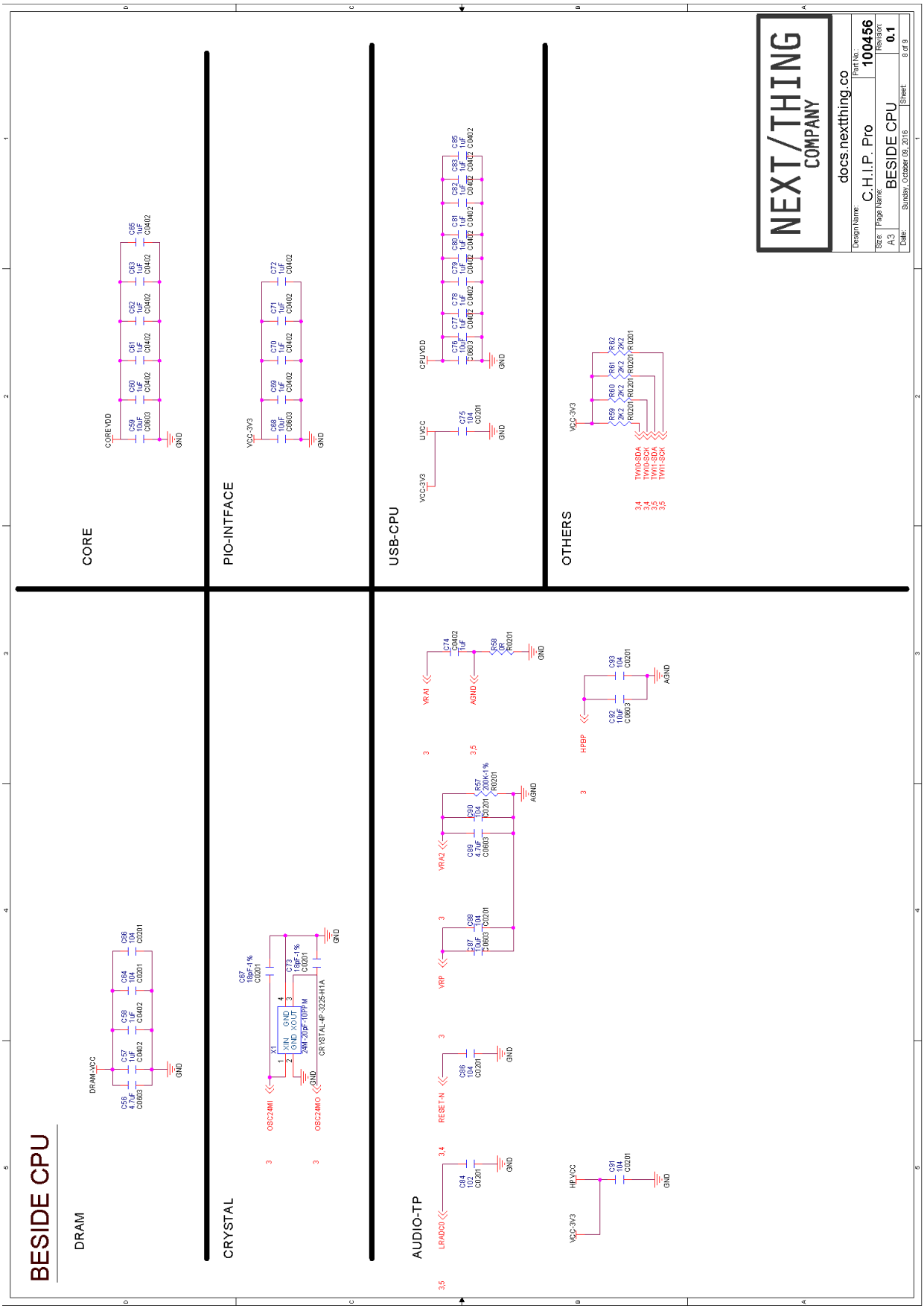


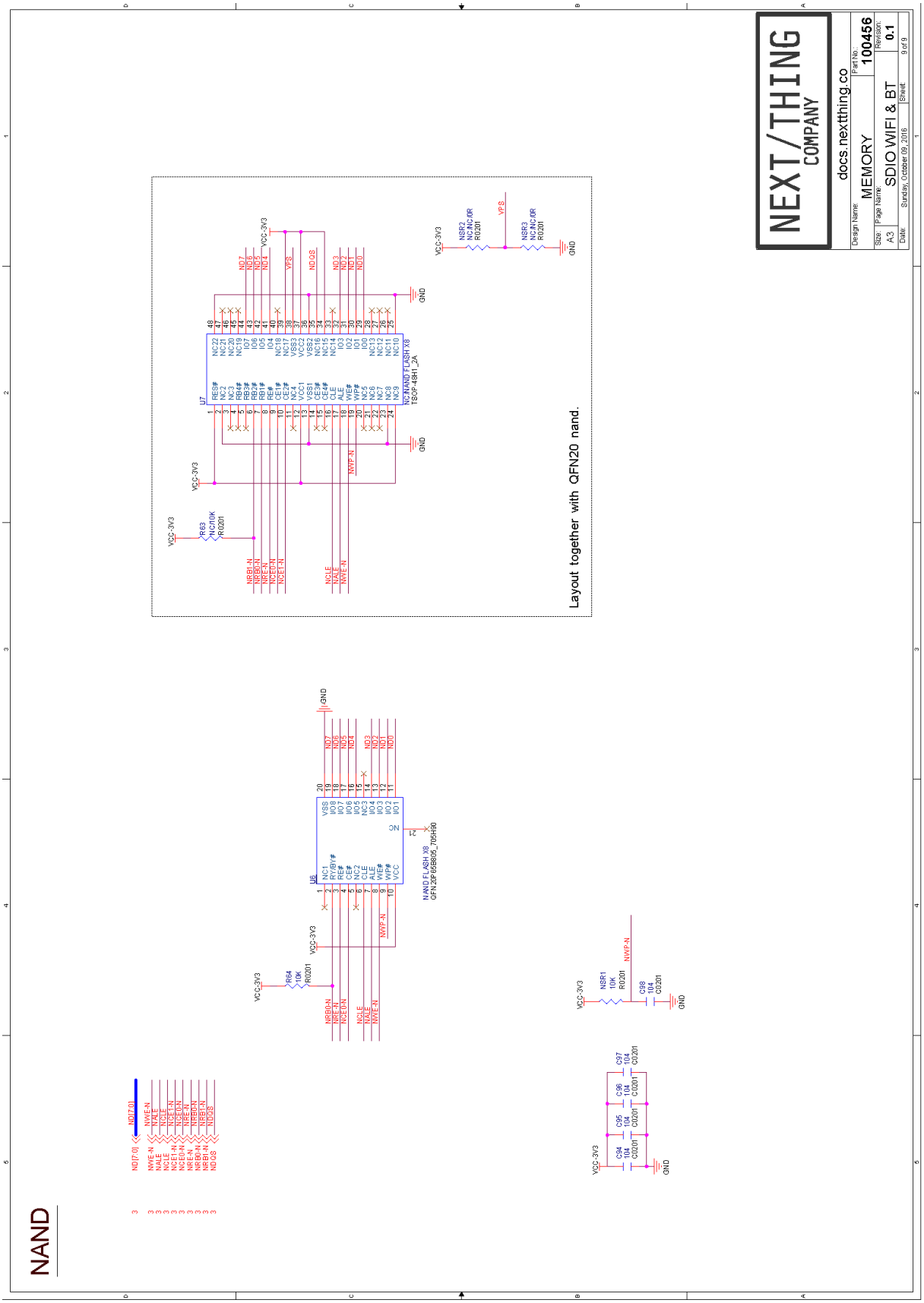












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